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An RF Performance Sensitivity and Process Yield Model for MIMIC CAD Applications

MIMIC Program, Phase 3

Final Report

Program Manager: Dr. R.J. Trew
Electrical and Computer Engineering Department
North Carolina State University
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Contract No. DAAL01-89-K-0906-4

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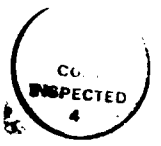

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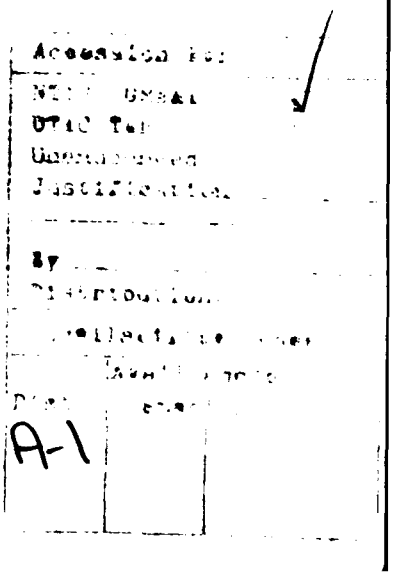

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R.J. Trew, D.E. Stoneking, P.Gilmore, C.T. Kelley, G.Bilbro

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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North Carolina State University
Raleigh, NC 27695-7911

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13. ABSTRACT *(Maximum 200 words)*

A physics based large-signal GaAs MESFET model and circuit simulator has been developed to predict and optimize the yield of GaAs MESFET designs before fabrication. Device acceptance criteria include both small- and large-signal RF operating characteristics such as small-signal gain, maximum power-added efficiency, and output power at 1dB gain compression. Channel doping details are described directly from processing specifications for material deposition, ion implantation, and implant annealing with the use of SUPREM 3.5, a process simulator developed at Stanford University. Monte Carlo techniques are used to estimate yield when disturbances in the MESFET parameters are modeled as multivariate Gaussian distributions. The yield estimator is integrated with an optimizer so that a design can be *centered* for maximum yield in the presence of process disturbances.

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Chapter 1

Introduction

The rapid development of the state-of-the-art in monolithic microwave integrated circuits has intensified the need to develop sophisticated CAD tools for use in device/circuit analysis and design. In particular, to increase the accuracy and effectiveness of CAD tools there is a need to develop device models based upon fundamental device physics. Active device simulators have improved rapidly in the last few years and now are being developed to the point where both accuracy and simulation efficiency are sufficient for practical 'first pass' design applications, that is device/circuit designs which initially prove successful.

In order to obtain the maximum benefit from a device simulator, the device model should be capable of describing the performance of a device before fabrication. In this manner the link between the process and RF simulators would be closed, and much time, effort, and expense would be saved since device optimization studies could be performed before the device is actually fabricated. This consideration indicates a physics based model, and the need to simulate RF operation indicates an efficient device algorithm based upon either analytic or table look-up techniques. Although a variety of physics based device models have been reported in the literature, most of the models in practical use are based upon equivalent circuit techniques (e.g., the MESFET models in TOUCHSTONE and SUPER-COMPACT) and require that the device be fabricated and characterized before the equivalent circuit can be established. This procedure does not allow process data to be used in a direct manner. Also, the proper definition of the equivalent circuit requires that a large number of devices be designed and fabricated in order to establish satisfactory and sufficient data bases. The accuracy of the equivalent circuit techniques is not well established, and much work remains to be done in developing suitable device characterization and parameter extraction techniques.

A physics based large-signal MESFET simulator suitable for use in microwave CAD has been developed at NCSU. With MIMIC Program, Phase 3, support the simulator has been significantly advanced and enhanced with an RF performance and process yield algorithm that allows the simulator to be used for both device design and process yield optimization. The resulting simulator is state-of-the-art and allows, for the first time, the physical design of MESFETs to be optimized so that a maximized percentage of devices will pass a specified yield criterion based upon large-signal performance such as RF output power, gain, power-added efficiency, etc. The yield simulator defines RF performance in terms of the physical design parameters actually accessible in the manufacturing process. The simulator

has proved to be both quantitatively as well as qualitatively accurate for use in MIMIC simulations, including both discrete MESFET devices and complete integrated power amplifier circuits.

The development of the simulator has been facilitated by interaction with Phase 1, MIMIC Program participants. In particular, experimental data has been supplied by ITT, Raytheon, Texas Instruments, General Electric, and Hughes. Access to this data has proved extremely valuable in guiding the development of the simulator so that it accurately predicts device performance. The simulator has been verified for accuracy against a variety of industrial devices, with varying channel doping and structural designs, operating under both class A and class B operating conditions. Examples of the verification tests are presented in Chapter 2 of this report.

Copies of early versions of the simulator and User's Manual have been delivered to MIMIC Program participants, including Raytheon, Texas Instruments, COMPACT Engineering, ITT, Martin-Marietta, General Electric, Hughes, TRW, Wright-Patterson AFB, and Fort Monmouth. The simulator and manual have been provided at no cost. In addition, user training has been provided to ITT and Raytheon.

The device model and verification are described in Chapter 2 of this report. The algorithms for computing large-signal performance measures and using them for sensitivity analysis, nominal performance optimization, and yield optimizization are presented in Chapter 3. In Chapter 4, the mathematical optimizer is detailed. Yield optimization experiments are given in Chapter 5, and Chapter 6 closes with conclusions.

Chapter 2

The Physical MESFET Model

The simulation philosophy guiding the NCSU simulator is indicated in the flow chart for an 'ideal' and integrated CAD procedure, as shown in Figure 2.1. As indicated in this chart a variety of models are required. The most significant factor is the desirability of interconnecting process, device, and circuit simulators so that a MIMIC can be simulated from process data (such as device geometry and channel doping details) all the way through to RF circuit performance. The availability of such an integrated simulator would allow, for example, a device design to be optimized based upon a desired RF performance specification (such as RF output power, gain, power-added efficiency, etc.).

Various building blocks for the 'ideal' procedure shown in Figure 2.1 are under development. A suitable process simulator (e.g., SUPREM 3.5) has been reported [1]. A version of SUPREM has been obtained from Stanford University and the code has been linked to the NCSU simulator (TEFLON). For ion-implanted devices the link between SUPREM and TEFLON permits channel doping details to be specified directly in terms of process parameters such as implant species, energy, dose, cap thickness, anneal time, etc.

Suitable microwave/mm-wave linear circuit simulators (i.e., the integrated circuit models indicated in Figure 2.1) have been intensively developed and are currently in a relatively advanced state (e.g., the commercially available simulators TOUCHSTONE and SUPER-COMPACT). These simulators also include versions of the passive element models indicated in Figure 2.1. The linear circuit models generally work fairly well and are extensively used by industry. In TEFLON, commercial simulators are used to determine characteristics for necessary passive elements.

2.1 Physical Device Models

Accurate device models suitable for use in microwave CAD simulators can be formulated from knowledge of the device's physical operation. These models are derived from solutions to a set of the basic semiconductor device equations [2, 3], subject to appropriate boundary conditions determined by the MESFET geometry and doping profile. The main difficulty in applying physical device models to microwave CAD simulators is the trade-off between accuracy and the large execution times generally required. Most of the physical models solve the semiconductor device equations using some form of numerical technique such as finite differences [4, 5] or finite elements [6]. The models can be formulated with varying complexity,

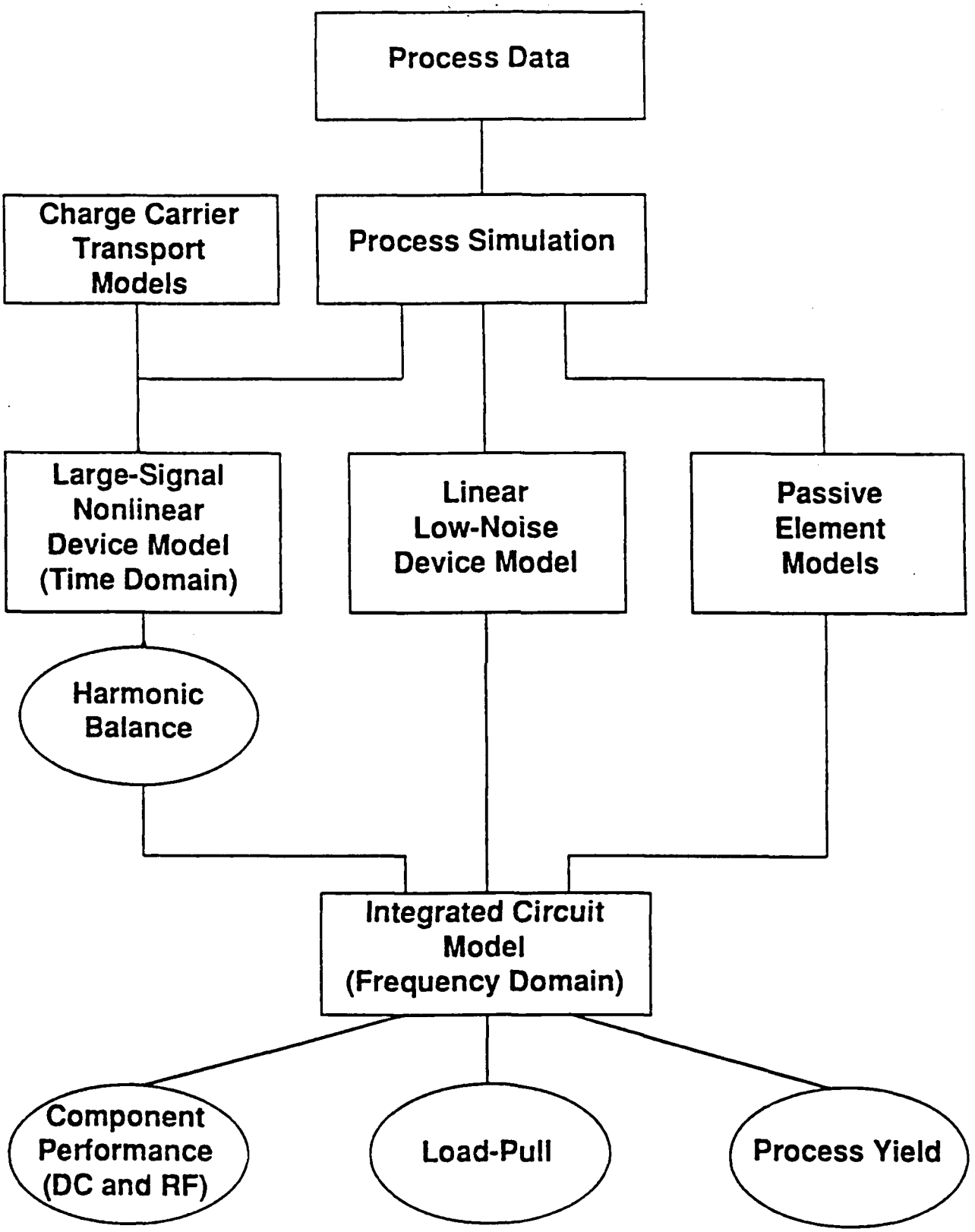


Figure 2.1: Components of an 'ideal' microwave/mm-wave integrated circuit computer aided design system.

depending upon the operational detail included. For example, the drift-diffusion approximation [5] where the charge carriers are assumed to be in thermal equilibrium with the crystal lattice is often assumed for devices with gate lengths on the order of a micron and greater and operating through X-band. This type of model has proved very valuable in illuminating operational physical phenomena. More advanced formulations include energy-momentum relaxation phenomena to account for nonequilibrium effects that become significant for submicron gate dimensions and very high frequency operation [7]. In these formulations the free electrons are not in thermal equilibrium with the crystal lattice over at least a portion of the conducting channel. Nonequilibrium effects tend to be most important at low bias where the majority of the carriers are in the low effective mass conduction band central valley. As bias or RF terminal voltage is increased the carriers transfer to higher conduction band valleys where higher effective mass tends to dampen the hot electron behavior. As a result, hot electron phenomena is reduced for power devices operated in saturation where the terminal voltages have large magnitudes.

Quantum effects can be included for devices such as HEMTs by including Schrodinger's equation in the set of semiconductor equations [8]. Solutions of this type tend to be complex and require extensive computer time to obtain solutions. The models have not yet been developed to the point where they can be efficiently used to simulate the RF performance of a device. In general, nonequilibrium phenomena can be simulated using hydrodynamic [9], numerical [7], or Monte Carlo [10] solution techniques. These models are very useful for investigating in precise detail the physical operation of the device. However, simulation time increases rapidly with model complexity and practical operation of the models is usually limited to *DC* solutions. *Large-signal operation such as transient performance* is generally investigated by performing a series of DC simulations for varying electrode potential. There have been a few attempts at using the numerical formulations to investigate the RF operation of a device [11, 12]. Conceptually, there is no reason that these models could not be applied to RF simulations, given sufficient computer resources. Such simulations are, however, beyond the current state-of-the-art.

Hybrid approaches in which a simplified version of the numerical formulation is coupled with an equivalent circuit approach have been presented [13, 14]. These models offer improved accuracy compared to the simple equivalent circuit models and provide a link between the numerical simulations and RF circuit simulators. The basic model, however, remains based upon numerical techniques which, in practice, limits the designer's flexibility to perform device and circuit optimization studies where large numbers of simulation runs are required. For example, every time the RF circuit is tuned a complete re-calculation is required. Since many tuning conditions are required to determine optimum circuit conditions simulation time quickly becomes unmanageable.

Solution of the device equations completely by analytic methods provides a good compromise between model accuracy and execution time [15, 16]. In this approach equivalent circuits are never used since the basic model, due to efficient analytic formulation, can be solved directly. When this approach is coupled with table look-up techniques execution time can be on the same order of magnitude or less than that required for the equivalent circuit models. Since device nonlinearities are inherent in the basic semiconductor equations it is not necessary to make a priori assumptions as to the form or identity of model nonlinear functions. The basis for the model is the device geometry, channel doping details, and bias

and RF operating conditions. The model is well suited for both device and RF circuit optimization studies. Application of the technique to RF performance and process yield optimization is attractive since large numbers of simulations can be efficiently performed.

2.2 The NCSU Microwave MESFET Simulator (TEFLON)

The NCSU physical GaAs MESFET simulator (TEFLON) is based upon efficient, analytic solution of the basic semiconductor device equations. The device model is quasi-static and is based upon an analytic formulation of the charge dipole domain [15, 16]. This formulation has, in turn, resulted in the derivation of a self-consistent large-signal analytic MESFET model that can easily be implemented in microwave CAD simulators. The time domain analytic device model is interfaced with an RF circuit by means of the harmonic balance method to produce an efficient and accurate nonlinear device/circuit microwave simulator.

The model permits the RF performance of a device or integrated circuit to be determined as a function of process and device design information and/or bias and RF operating conditions. In this manner a complete integrated device/circuit simulator, as indicated in Figure 2.1, is possible. Such an integrated simulator allows both the active device and the passive elements to be optimized, based upon the parameters accessible in the fabrication process. That is, factors such as device geometry, ion-implant species, dose, and energy that result in optimized RF output power, power-added efficiency, etc. can be determined. This approach eliminates the need to experimentally characterize the devices in order to parameter extract equivalent circuit element values. The experimental measurements that are of interest consist of RF performance data such as Pout vs. Pin, PAE, gain, spectrum, and impedance. This data can be directly compared to simulated data to verify the model. Once verified, the model can then be used in the design process.

A block diagram for the NCSU large-signal, analytic model indicating the information flow is shown in Figure 2.2. The inputs can be supplied from experimental measurements or calculated data. The outputs of the simulator consist of DC I-V characteristics, small-signal parameters, and large-signal data. A major advantage of this type of simulator is that the DC and RF performance of the device can be determined as a function of parameters that are actually accessible in the fabrication process.

2.3 Verification Experiments

In practice, the simulator is currently limited to single device circuits operating in the common-source configuration, as shown in Figure 2.3. Any arrangement of source and load impedances, and parallel or series feedback networks can be accommodated. The common-source limitation is not fundamental and was implemented for convenience. The simulator could be generalized with slight modifications to the code. However, this has not been done due to time restrictions.

The simulator requires that channel doping details be known. The data can be calculated from process models (e.g., SUPREM 3.5 [1]) or determined from measurements. In order

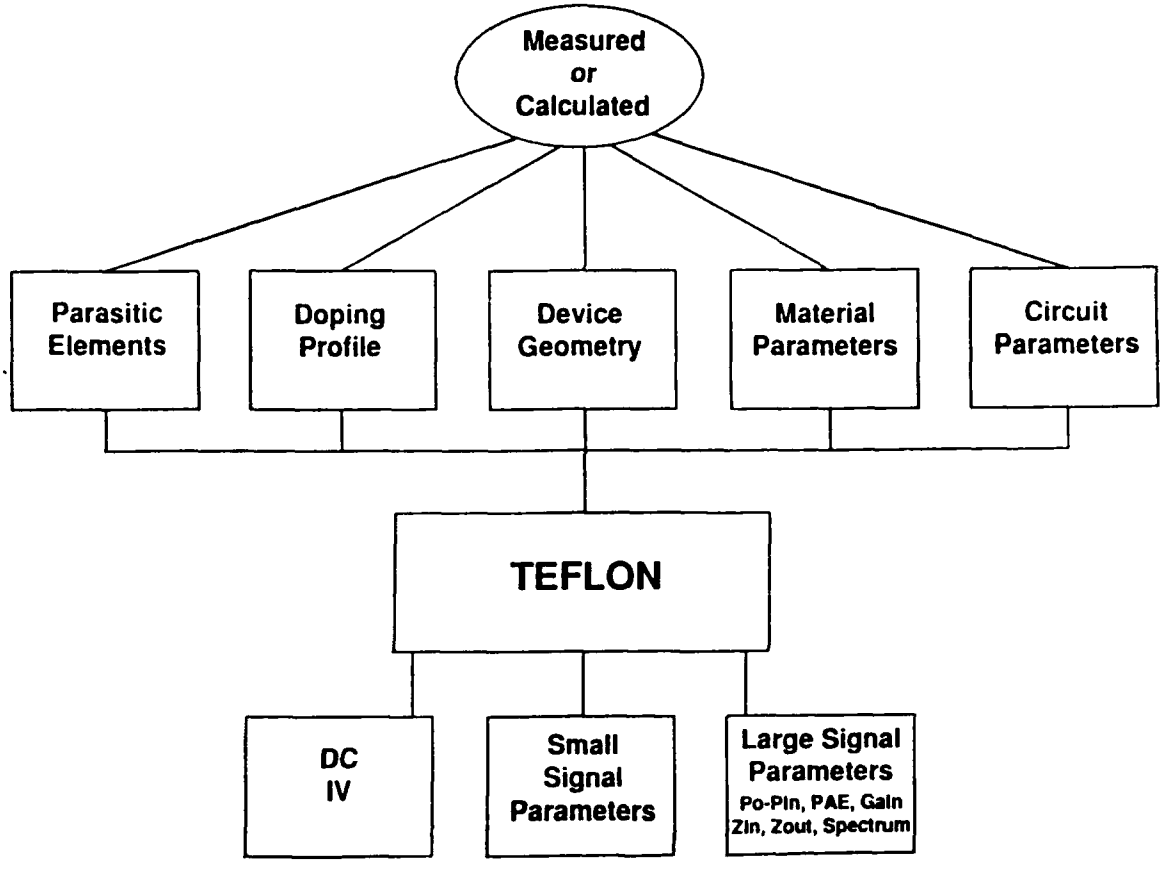


Figure 2.2: Information flow for the NCSU large-signal model (TEFLON).

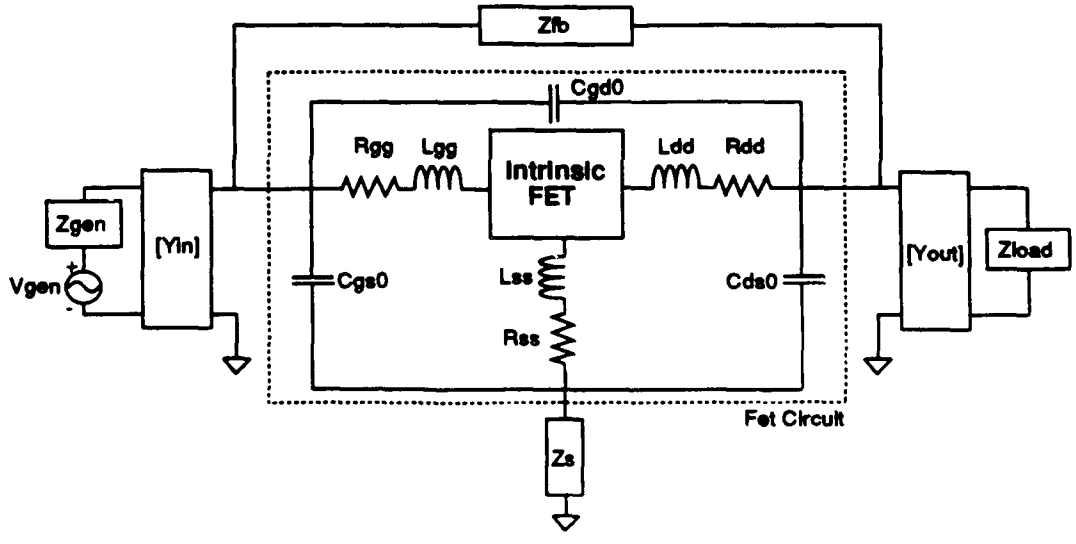


Figure 2.3: The complete TEFLON RF circuit schematic.

to facilitate determination of the doping profile, a parameter extraction technique has been developed. The parameter extraction technique automatically adjusts, by means of a mathematical optimization procedure, the magnitude of the physical parameters in the model until good agreement between a variety of performance characteristics are obtained. Typically, these consist of the drain and gate currents in addition to RF output power, PAE, and gain. The parameter extraction routine has proved valuable in matching simulator performance to measured data.

In Figure 2.5 is an example of applying the simulator to a specified device structure with the theoretical doping profile is shown in Figure 2.4. The device was a C-band MESFET fabricated by ITT. The device has a gate length of 1 micron and a gate width of 2.5 mm. The specified doping profile was used and the parasitics and electron velocity-field characteristic were adjusted until the simulated DC I-V characteristics were in agreement with the measured data. As indicated in Figure 2.5, excellent agreement was obtained. In order to match the experimental data the velocity-field characteristic for GaAs is used as the 'fitting' parameter. The low field mobility can be taken from measured data or varied until good agreement between the measured and simulated I-V characteristic in the linear region is obtained. For doping densities in the range of $10^{17}cm^{-3}$ the mobility is usually in the range 2000-4000 $cm^2/V \cdot sec$. The saturated velocity is adjusted until the model predicts the correct open channel current (I_{dss}). Typically, for a one micron gate length device, the saturated velocity is in the range of $1.4 - 1.6 \times 10^7$ cm/sec. The saturated velocity scales inversely with gate length, as expected.

Simulations of the class A RF operation of the device at 5.5 GHz produced the results shown in Figure 2.6. As indicated, excellent agreement between the measured and simulated performance is obtained. The simulator accurately predicts the RF output power, power-added efficiency, gain, and DC drain current, over a range of input RF power sufficient to drive the device better than 6 dB into saturation. Of particular note is the agreement between the measured and simulated PAE. This performance function is typically difficult to match using commercially available equivalent circuit models.

An example of use of the parameter extraction algorithm is shown in Figure 2.7. This device has a 0.5 micron gate length and a 1 mm gate width and was operated class A at 10 GHz. The specified implant profile was used as the initial doping profile. The optimizer varied the doping profile, velocity-field characteristic, and parasitics until good agreement between the measured and simulated performance was obtained. Again, excellent agreement between the measured and simulated data was obtained. As indicated in the doping profile plot, the free electron density varies from the implanted donor profile. As expected, due to diffusion effects, the free electron distribution is reduced near the implant peak, but is increased as the implant 'tails' into the substrate. Also of significance are the variations in the drain and gate currents as the device is driven into saturation. Accurate modeling of the saturation mechanisms is of first order importance to obtaining good results. It has been determined that saturation in MESFETs occurs due to forward and reverse conduction of the gate electrode. This will be discussed in more detail later in this section.

Two other ion-implanted devices operating at 10 GHz were simulated and the results obtained are shown in Figures 2.8 and 2.9. Again, excellent agreement between the measured and simulated data is obtained. Devices from ITT, Raytheon, Texas Instruments, General Electric, and Hughes have been simulated. The devices had gate lengths ranging from

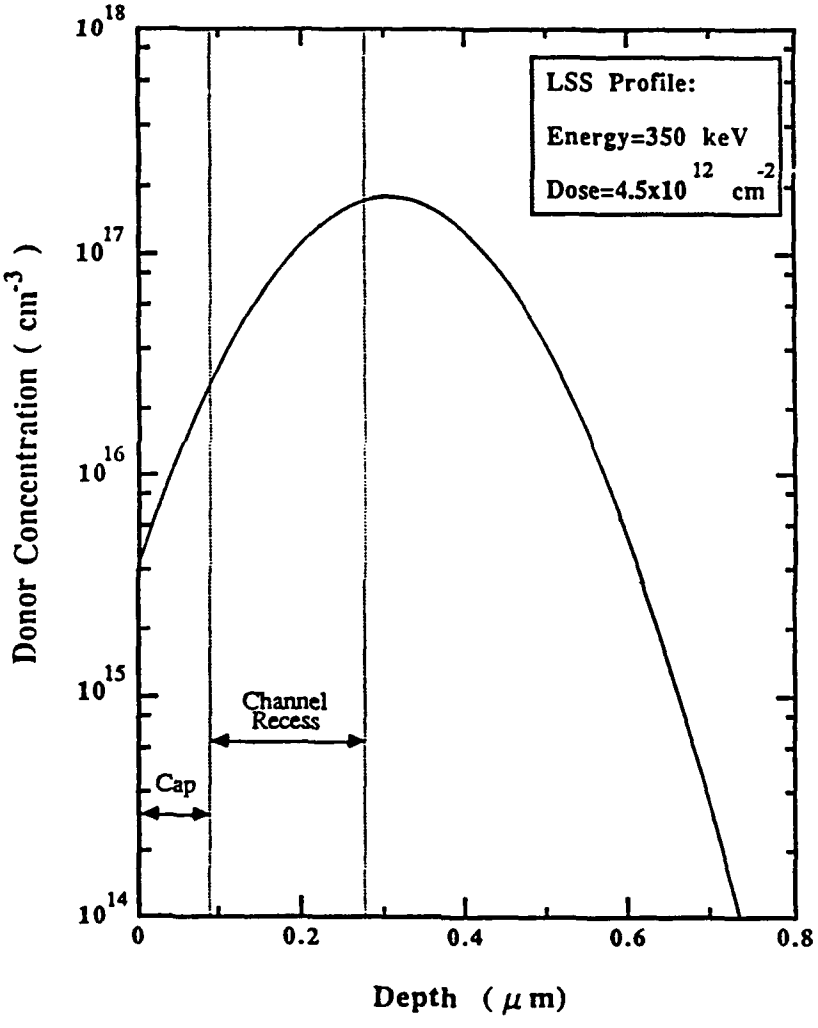


Figure 2.4: Modeled doping profile for the 2.5 mm C-band MESFET.

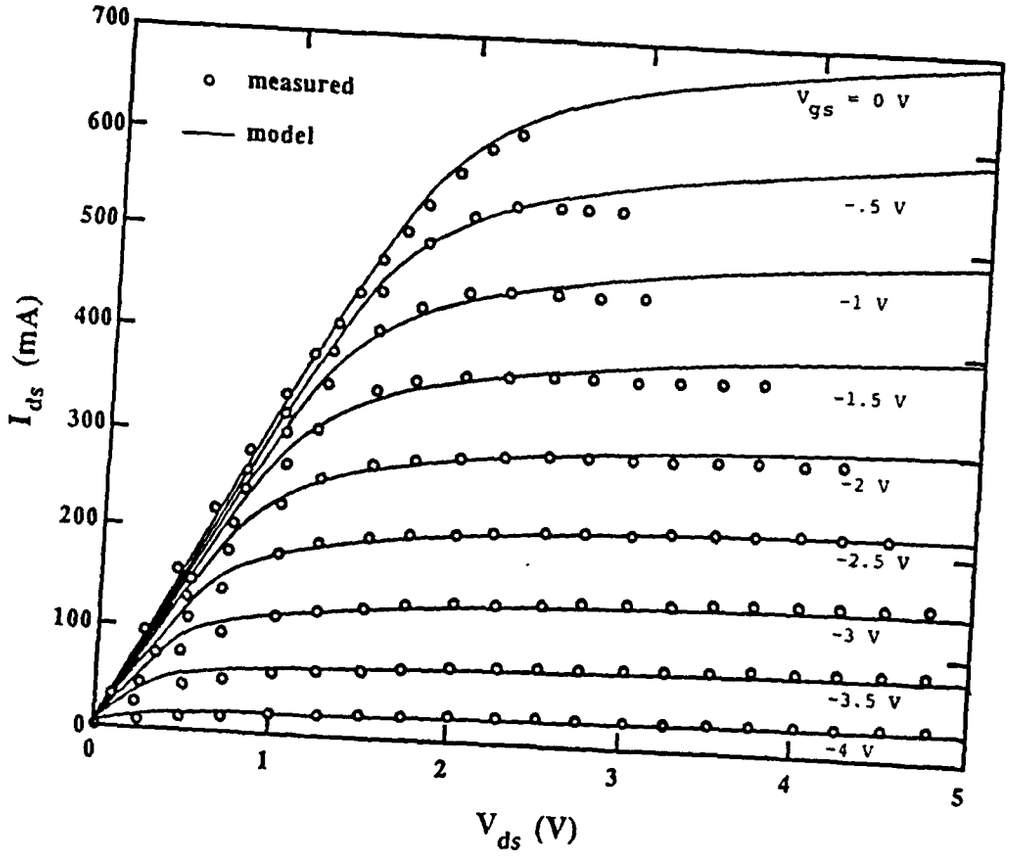


Figure 2.5: Measured and modeled static I-V characteristics of the 2.5 mm C-band MESFET.

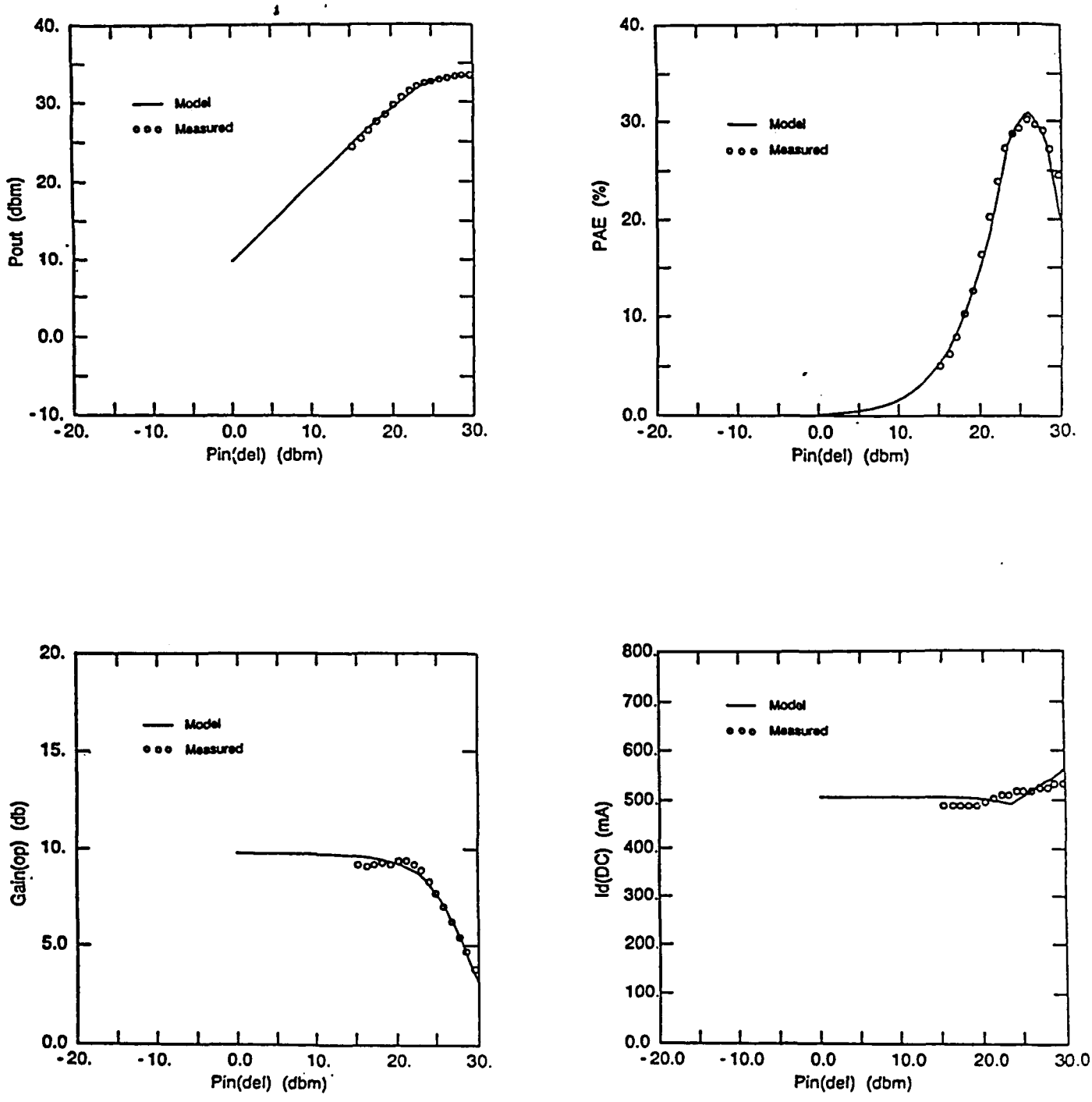


Figure 2.6: ITT MSAG MESFET - Measured and simulated performance (L_g = 1 μm, W_g = 2.5 mm, V_{ds} = 10 V, I_{ds} = I_{dss}/2, F = 5.5 GHz)

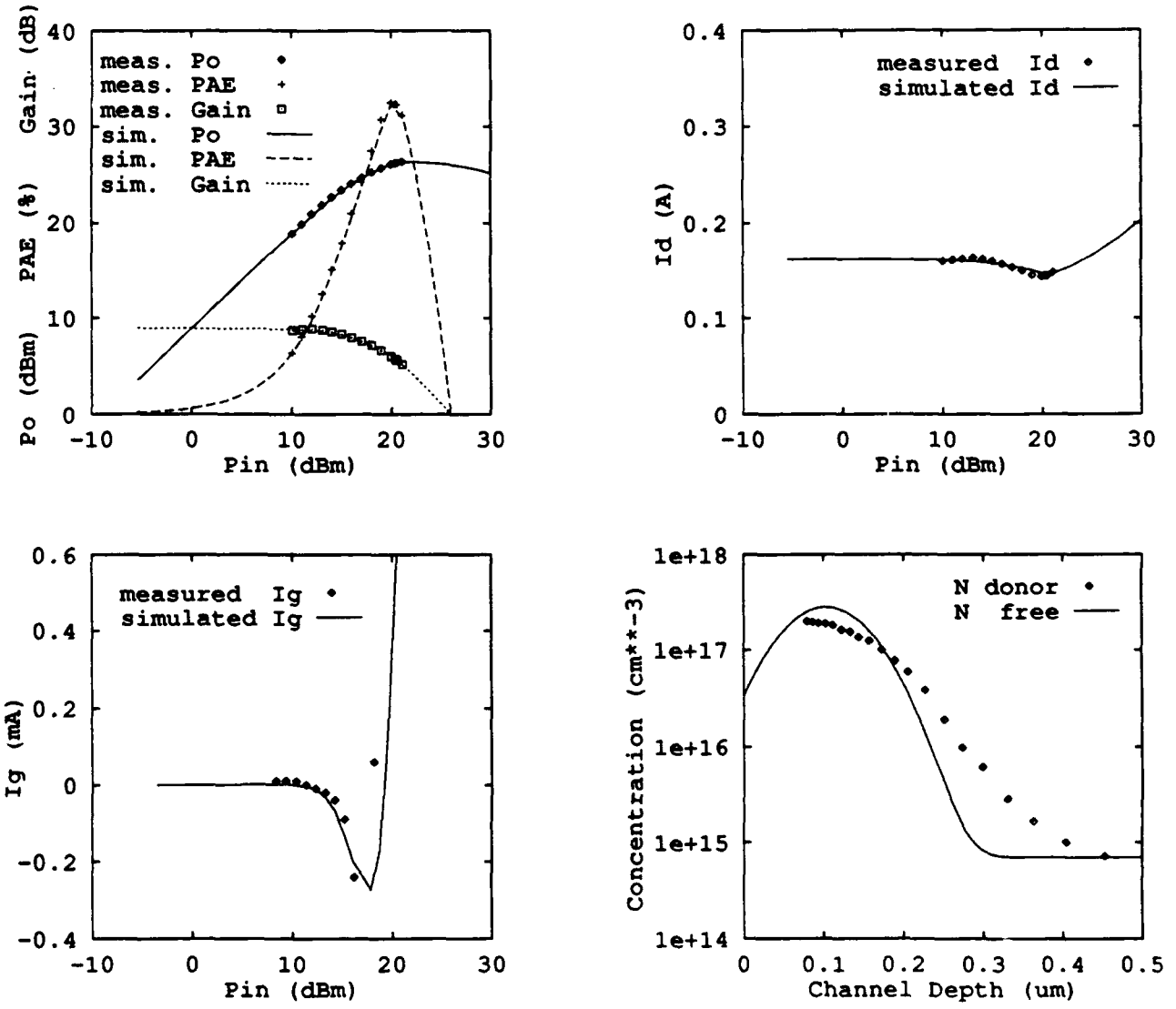


Figure 2.7: Parameter extracted RF and doping results

0.25 micron to 1 micron and gate widths ranging from 0.5 mm to about 4 mm. Both ion-implanted and buried channel (i.e., low-high-low) doping profiles were simulated. The devices were designed for operation at C and X-bands. In addition, complete integrated amplifiers fabricated by ITT were simulated, also with good results. Good agreement between the simulated and measured data has been obtained in all cases.

2.4 Saturation in MESFETs

The excellent agreement between the measured and simulated DC and RF performance results from accurate modeling of the primary saturation mechanisms in MESFETs. Investigation of saturation in these devices indicates that saturation occurs when the gate electrode is driven into reverse and forward conduction. This is indicated in Figure 2.10, which shows plots of the dynamic v-i locus superimposed upon the DC I-V characteristics for a typical 0.5 micron gate length, 1 mm gate width MESFET operating class B. The dynamic v-i loci are shown for operation in the linear region and when the device is driven 3 dB into saturation. When operating in the linear region the dynamic locus is essentially elliptical, except when it is clipped due to the class B conditions. As saturation is achieved, the dynamic terminal RF voltage exceeds the gate breakdown voltage and gate current flows. The terminal voltage decreases until it gains sufficient magnitude to produce forward conduction on the reverse portion of the RF cycle.

When operating in saturation these two mechanisms compete. That is, reverse breakdown and forward conduction occur during each RF cycle. Which mechanism dominates is determined by the device structure, bias, and RF tuning conditions. This is illustrated in Figure 2.11, which shows real-time waveforms at the gate and drain terminals for a 0.5 micron gate length device operating class A at 10 GHz. The solid lines indicate increasing levels of RF drive, varying from small-signal linear operation to about 3 dB into saturation. As shown, linear operation produces sinusoidal terminal waveforms. As the device is driven into saturation, significant waveform clipping occurs. The waveform distortion is primarily due to the gate conduction characteristics, as indicated in the two plots at the bottom of the figure. In this particular device, forward gate conduction is dominant, although reverse breakdown conduction of the gate electrode is also clearly seen.

Reverse breakdown of the gate electrode is dominant in determining the drain voltage at which the device can be operated. Typically, for optimum performance MESFETs can only be biased at about 40-50% of the drain-source breakdown voltage due to the saturation mechanism. If the breakdown voltage is low, sufficient drain bias to operate the device efficiently can not be applied and performance suffers. The RF output power that can be obtained is essentially linearly dependent upon drain bias. High breakdown voltage is, therefore, of fundamental importance in obtaining maximum RF performance from MESFETs.

Accurate simulation of the DC and RF performance of MESFETs requires that accurate models for gate conduction be formulated. Breakdown in MESFETs, however, is not well understood and an accurate model that predicts observed breakdown phenomena has not previously been reported.

Gate-drain breakdown must be accurately simulated if good agreement between modeled and experimental data is to be obtained. Unfortunately, most models for reverse gate

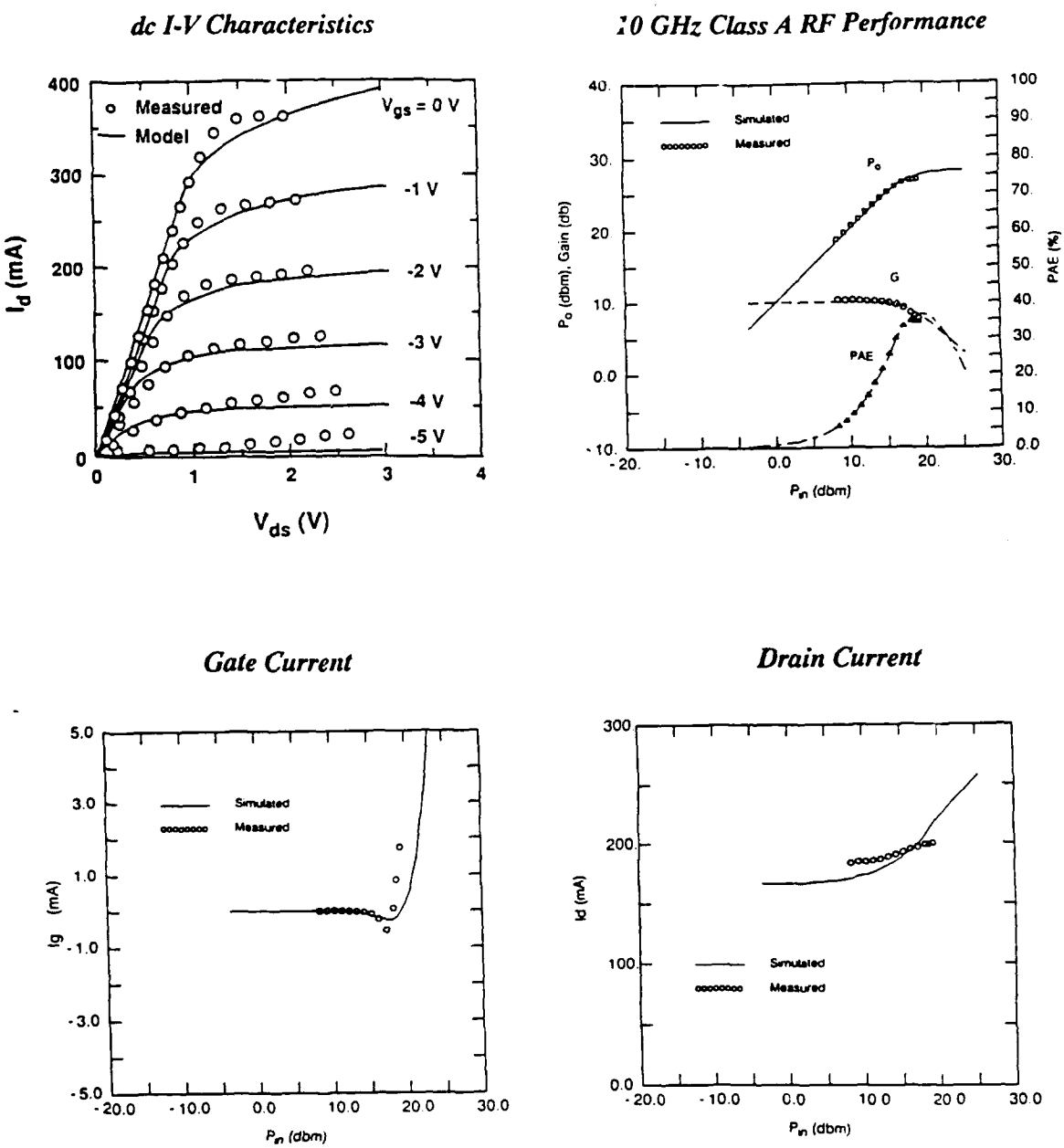


Figure 2.8: Measured and simulated GaAs MESFET performance ($L_g = 0.5\ \mu m$, $W_g = 1.25$ mm)

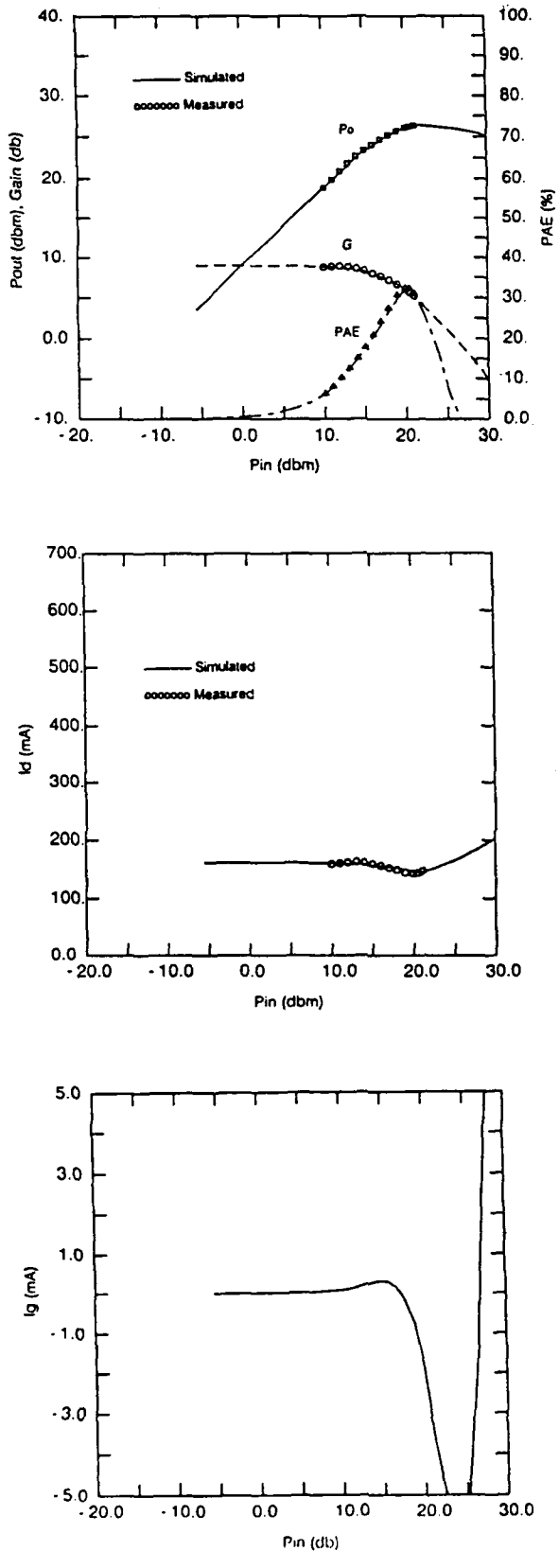


Figure 2.9: Measured and simulated GaAs MESFET performance ($L_g = 0.5\ \mu m$, $W_g = 1.125$ mm, f = 10 GHz, Class A)

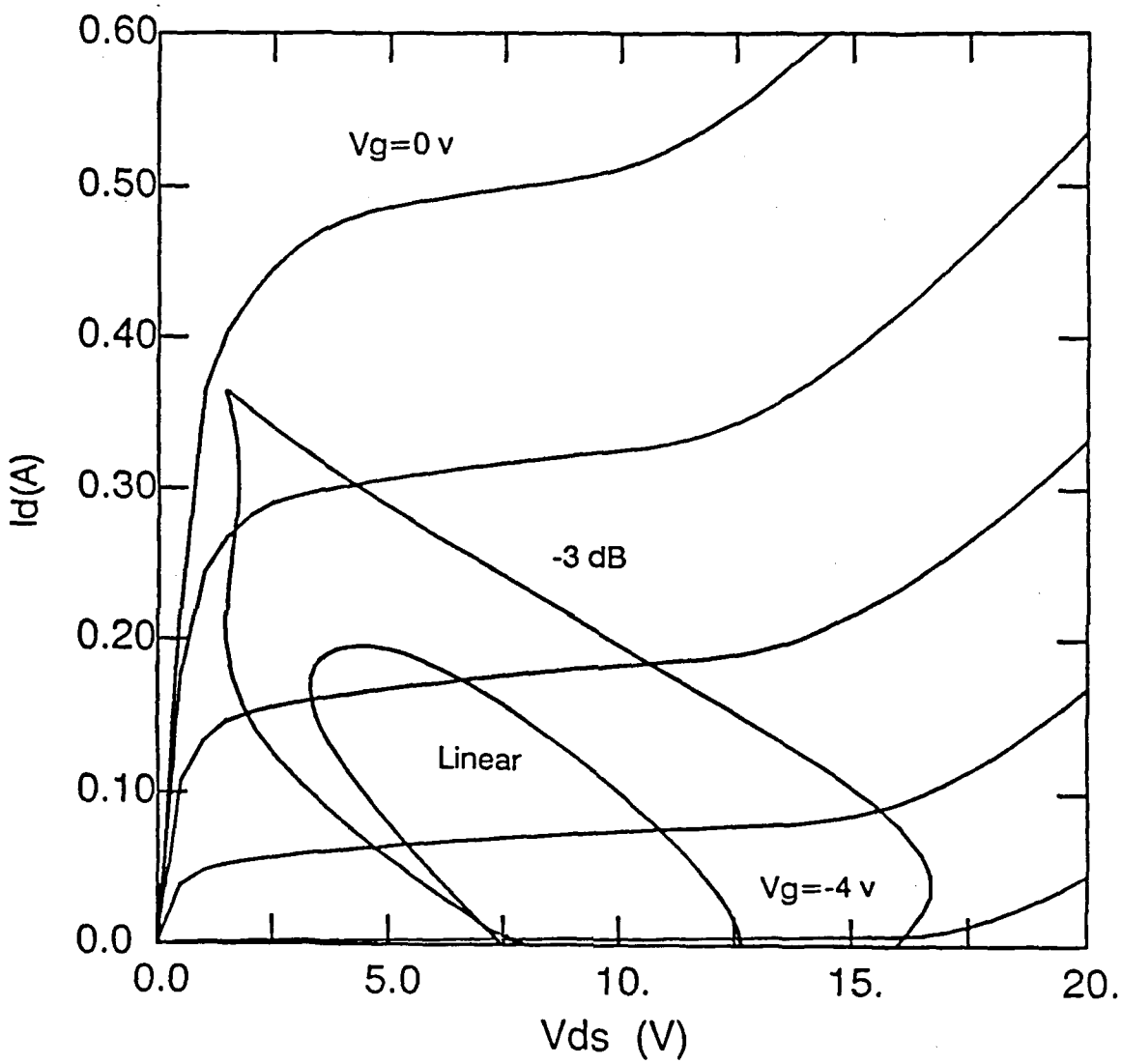


Figure 2.10: Dynamic and DC I-V characteristics for a MESFET ($L_g = 0.5\ \mu m$, $W_g = 1$ mm, f 10 GHz, Class B)

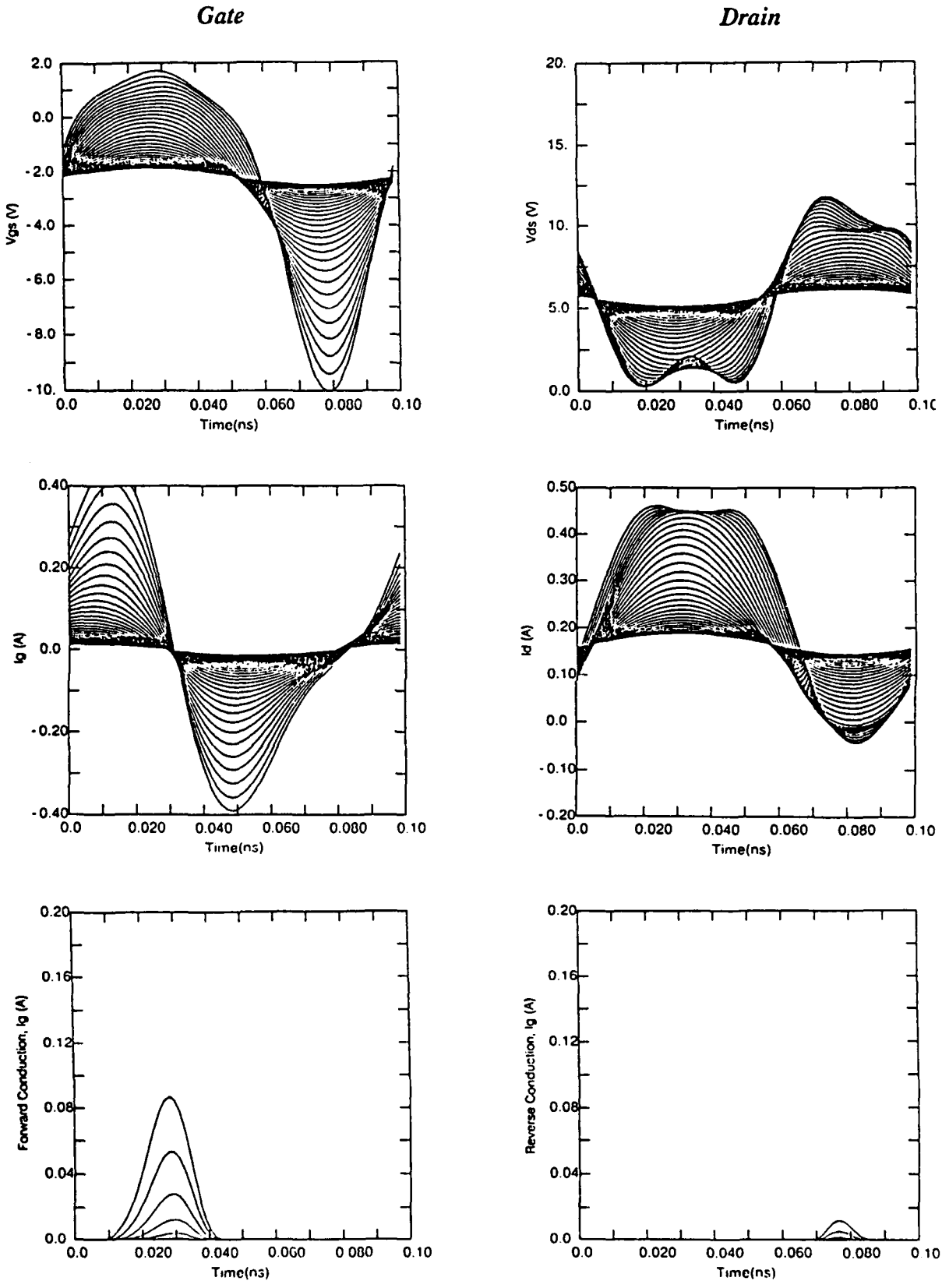


Figure 2.11: MESFET real time waveforms (L_g = 0.5 μm, W_g = 1 mm, Class A, f = 10 GHz)

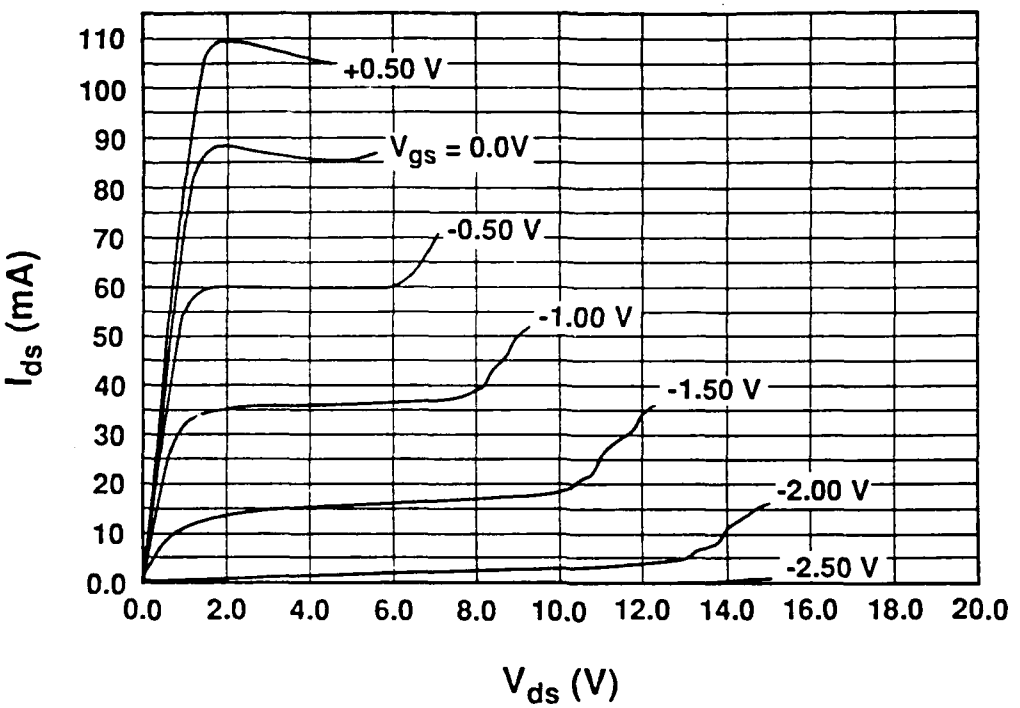


Figure 2.12: I-V characteristics showing drain-source breakdown for ion-implanted GaAs MESFET (L_g = 0.5 μm, W_g = 300 μm).

breakdown in GaAs MESFETs do not yield results in agreement with measured data. In particular, the models do not correctly predict the increasing breakdown voltage versus gate bias shown in Figure 2.10 and commonly measured in experimental data, as indicated in Figure 2.12. The data shown in Figure 2.12 were measured for an ITT MSAG MESFET. The ability to simulate this behavior is, of course, fundamental to obtaining accurate simulator results. We have proposed a mechanism for gate breakdown in MESFETs that will yield a breakdown model suitable for incorporation into microwave CAD simulators [17]. The mechanism has been verified with experiment [18]. A simplified and qualitative version of this model is partially responsible for the excellent simulated results presented here by accurately including RF saturation due to gate conduction. The model, for the first time, correctly predicts the increasing gate-source breakdown voltage as gate bias is increased towards pinch-off, in agreement with the measured data shown in Figure 2.12. The gate conduction model allows for both forward and reverse breakdown conduction of the gate electrode and permits calculation of conduction during the RF cycle, as shown in Figure 2.11.

Chapter 3

Large-Signal Analysis and Optimization of Power Amplifiers

A number of algorithms were added to the simulator to calculate large-signal performance measures applicable to MESFET power amplifiers. These large-signal performance measures were then used as the basis for sensitivity analysis, nominal performance optimization, and yield optimization. These components are discussed in this chapter with the exception of the mathematical optimization algorithm, which is the topic of Chapter 4.

3.1 Calculation of Performance Measures

Three classes of performance measures are available: small-signal gain, measures associated with gain compression levels, and measures associated with maximum power-added efficiency. Each of these classes has two subclasses. The first subclass consists of transducer quantities, and the second subclass comprises operational quantities. The difference between the two subclasses will be developed below.

The small-signal transducer gain, G_t, is given by:

$$G_t = \frac{1}{4}\sum_{k=1}^{4}\left(P_{l,dB}^{k} - P_{g,dB}^{k}\right).$$

Where $P_{g,dB}$ is the RF power in dBm available from the generator Vgen shown in Figure 2.3 and $P_{l,dB}$ is the RF power in dBm delivered to the load. The four values of $P_{g,dB}$ are specified by the user, and they must be in the small-signal regime. The small-signal transducer gain has no other associated performance measures.

Similarly, the small-signal operational gain, G_o, is given by:

$$G_o = \frac{1}{4}\sum_{k=1}^{4}\left(P_{l,dB}^{k} - P_{i,dB}^{k}(P_{g,dB}^{k})\right).$$

Where $P_{i,dB}$ is the input power delivered by the generator to the circuit. The user must supply four values for $P_{g,dB}$ that are all in the small-signal regime. Given these values of $P_{g,dB}$, the simulator calculates $P_{l,dB}$ and $P_{i,dB}$. The small-signal operational gain has no other associated preformance measures.

The transducer gain compression measures result from solution of

$$(P_{l,dB}(P_{g,dB}) - P_{g,dB}) - (G_t - G_C) = 0 \qquad P_{g,dB} \in R.$$

Where G_t is computed by the formula above and G_C is a gain compression level in dB. G_C is user selectable as 1, 3, or 6 dB. The Van Wijngaarden-Dekker-Brent root finding algorithm [19] is used to solve the above equation. Once the root of the equation is found, the available performance measures are $P_{g,dB}$, $P_{l,dB}$, and the gain-output power product $(2P_{l,dB} - P_{g,dB})$ at the solution.

The operational gain compression measures result from solution of

$$(P_{l,dB}(P_{g,dB}) - P_{i,dB}(P_{g,dB})) - (G_o - G_C) = 0 \qquad P_{g,dB} \in R.$$

Where G_C is the selectable gain compression level and G_o is computed by the previously given formula. Again, the Van Wijngaarden-Dekker-Brent root finding algorithm [19] is used. Once the root of the equation is found, the available performance measures are $P_{i,dB}$, $P_{l,dB}$, and the gain-output power product $(2P_{l,dB} - P_{i,dB})$ at the solution.

The final class of performance measures result from maximizing expressions for the power-added efficiency. The maximum transducer power-added efficiency is determined as

$$\max_{P_g}\{\mathrm{PAE}_t\} = \max_{P_g}\left\{\frac{P_l(P_g) - P_g}{P_{DC}(P_g)}\right\} \qquad P_g \in R$$

where P_l is the RF power in mW delivered to the load, P_g is the RF power in mW available from the generator, and P_{DC} is the DC power in mW delivered to the transistor. Brent's method [19] is used to perform this 1-D optimization. The transducer performance measures are the maximum PAE_t and P_g, P_l, P_l/P_g, and P_l^2/P_g at the maximum.

The maximum operational power-added efficiency is defined as

$$\max_{P_g}\{\mathrm{PAE}_o\} = \max_{P_g}\left\{\frac{P_l(P_g) - P_i(P_g)}{P_{DC}(P_g)}\right\} \qquad P_g \in R$$

Brent's method [19] is used to maximize the operational power-added efficiency expression. The operational performance measures are the maximum PAE_o and P_i, P_l, P_l/P_i, and P_l^2/P_i at the maximum.

To calculate the performance measures the user must specify the DC bias for the device. The program supports eight different bias modes — four ways of setting the gate-source bias voltage and two ways of setting the drain-source bias voltage. The user's options for specifying the gate-source and drain-source bias voltages are summarized in Table 3.1.

While calculating a performance measure a number of situations can arise where the measure become invalid for some reason. These situations are dealt with by penalizing the measure under consideration. The linear value of the measure is set to either zero or 1×10^{-20}. A zero value is used if the linear value is never converted into a logarithmic representation. Otherwise, the value of 1×10^{-20} is used. The circumstances leading to penalization of the performance measures are enumerated below:

1. When computing gain compression or maximum power-added efficiency performance measures, the measure is penalized if the gain at the root or maximum becomes less than 1 dB, or some other user specified value.

$V_{GS} = a$	User specifies a
$V_{GS} = bV_{po}$	User specifies b
$I_{DD}(V_{GS}) = c$	User specifies c
$I_{DD}(V_{GS}) = dI_{DSS}$	User specifies d
$V_{DS} = e$	User specifies e
$V_{DS} = fV_{dsbd}$	User specifies f

Table 3.1: Bias modes available when calculating performance measures

2. The performance measure is penalized when the device's pinch-off voltage fails to fall on a user specifiable interval, which defaults to -15 V to -1 V.

3. When the DC bias does not lie in the valid region of the $V_{gs} - V_{ds}$ plane, the performance measure is penalized. The valid region is given by the following relationships:

$$\begin{array}{rcll} V_{gs} & \geq & AV_{po} & \text{default } A = 0.95 \\ V_{gs} & \leq & BV_{po} & \text{default } B = 0.1 \\ V_{ds} & \geq & CV_{dsbd} & \text{default } C = 0.1 \\ V_{ds} & \leq & D\left[m_{bd}\left(V_{gs} - V_{po}\right) + V_{dsbd}\right] & \text{default } D = 1.0. \end{array}$$

   Where A, B, C, and D are user controls on the valid region, and m_{bd} is slope of the line in the V_{ds} - V_{gs} plane which marks the onset of gate-drain breakdown.

4. Alternatively, when the DC bias is specified as an invalid $I_{dd} - V_{ds}$ combination, the performance measure is penalized. The valid $I_{dd} - V_{ds}$ region is given by the following relationships:

$$\begin{array}{rcll} I_{dd} & \geq & EI_{dss} & \text{default } E = 0.05 \\ I_{dd} & \leq & FI_{dss} & \text{default } F = 0.95 \\ V_{ds} & \geq & CV_{dsbd} & \text{default } C = 0.1 \\ V_{ds} & \leq & D\left[m_{bd}\left(V_{gs} - V_{po}\right) + V_{dsbd}\right] & \text{default } D = 1.0. \end{array}$$

   Where E and F are user controls on the valid region.

5. The device and/or its embedding circuit are supplying RF power at the fundamental to the generator impedance (i.e., the transistor is oscillating.)

6. While evaluating yield estimates, any sample devices which fall outside of the disturbance hyperbox (see section of yield estimation) result in a penalized performance measure.

3.2 Large-Signal Sensitivity Analysis

The first application of these performance measures was large-signal sensitivity analysis. The sensitivity is given by the following formula:

$$S_p^m = \frac{p}{m}\frac{\partial m}{\partial p}$$

where m is the performance measure and p is the parameter under study. The performance measures available are all those listed in Section 3.1. The parameters include all the MESFET model parameters and all parameters of the circuit blocks Z_{gen}, Z_{load}, Z_s, and Z_{fb}.

The sensitvity is calculated numerically within TEFLON by evaluating the performance measure at a sequence of user specified parameter values. This sequence of data points is then splined with a Hermite polynomial spline. The spline is programmed to return interpolates of both the function and its derivative. The derivative interpolates are multilied by their corresponding normalization factors p_i/m_i to give the sensitivity.

Sensitivity analysis is useful for determining which device or circuit parameter fluctuations cause the greatest changes in critical performance measures. This knowledge is useful in several ways. Once a nominal set of device and circuit parameters is selected, sensitivity analysis allows assignment of parameter tolerances such that the performance measures stay within specified bounds. Another application of sensitivity analysis is determining which device or circuit parameters to use during optimization runs.

Examples of sensitivity analyses for an ion-implanted device, a buried channel device, and uniform channel device are given in Appendices C, D, and E, respectively. These analyses were performed to selected the optimization variables used to generate the results presented in Chapter 5.

3.3 Nominal Performance Optimization

Mathematical optimization of a device design (i.e., a single unperturbed design) with respect to one of the above performance measures is nominal performance optimization. At present, nominal performance optimization is limited to a single measure per optimization run. Multiple performance measures could be used if a satisfactory method of combining them into a single number was selected and implemented.

The optimization algorithm employed is novel and was developed under this contract. It is a gradient based algorithm which can deal successfully with objective function noise and local minimum.

Nominal performance optimization can be a useful design tool, but often the resulting designs exhibit poor manufacturing yields. These poor yields result from the optimizer placing the design near a performance cliff [44, 42]. A more useful, but computationally more expensive, technique is yield optimization, which was the main effort under this contract and is the topic of the next section.

3.4 Yield Optimization

Computer aided design (CAD) has helped to improve process yields and the average performance of monolithic microwave integrated circuits (MMICs) through the application of statistical circuit design techniques. A principal statistical circuit design technique is yield optimization.

The yield optimization problem can be formulated two ways:

$$\max_{x} \left\{ Y(x) = \int_{R_A} p(v)dv \right\}$$

or

$$\max_{x}\left\{Y(x)=\int_{-\infty}^{\infty}p(v)\phi(x+v)dv\right\}$$

where $x \in R^n$, $p(v)$ is the parameter disturbance probability density function, and R_A is the acceptability region. The acceptance function $\phi(x+v)=1$ if $(x+v) \in R_A$. Otherwise. $\phi(x+v)=0$. The first formulation requires approximating the region of acceptability and leads to region of acceptability approaches. The second formulation is usually solved with Monte Carlo techniques.

A number of different authors proposed region of acceptability approaches. Scott and Walker [20] and Leung and Spence [21] pursued the regionalization method. Regionalization does a direct search on the space to determine the acceptability region. The simplicial approach was used by Director and Hachtel [22, 23, 24]. The simplicial approach approximates the region of acceptability with a polyhedron formed by points on the boundary. The design center is then the center of a hypersphere which is contained within the polyhedron. Bandler and Abdel-Malek [25, 26, 27] approximated the acceptability region with hyperboxes and linear cuts. The yield is estimated as the hypervolume of the region of acceptability divided by the hypervolume of the tolerance box. The multicircuit approach to modeling the region of acceptability was introduced by Bandler *et al.* [28] who used a group of circuit designs to approximate the region of acceptability. Bandler and Chen [29] then used generalized l_p centering to optimize yield. In generalized l_p centering, a l_p error function of the difference between each circuit's response and the acceptable region boundary is minimized.

Various other authors sought to solve the yield optimization problem with Monte Carlo techniques. Soin and Spence [30] advocated a center of gravity method. N Monte Carlo samples are taken. The centers of gravity of the passed and failed points are determined. The design center is then located by a line search along the line joining the centers of gravity. Stochastic optimization was used by Styblinski and Ruszczynski [31] and Kjellström and Taxèn [32]. In this approach, small sample Monte Carlo yield estimates are stochastically optimized. Singhal and Pinel [33] introduced parametric sampling. The parametric sampling technique reuses previous samples when forming a Monte Carlo yield estimate. The control variate technique [34] for reducing the Monte Carlo noise in the yield estimate was used by Hocevar *et al.* [35] and Soin and Rankin [36, 37]. Biernacki et al. [38] used efficient quadratic approximation. This technique approximates the circuit response with a multidimensional quadratic function which reduces the cost of the Monte Carlo samples. The approximation is generated from less than the minimum number of basis points by a maximally flat interpolation technique. Ellipsoids of decreasing volume were proposed by Abdel-Malek and Hassan [39]. This method approximates the region of acceptability with an ellipsoid which is determined by decreasing the volume, moving the center, and changing the shape of a starting ellipsoid. The design center is then center of the final ellipsoid.

In addition to the works already cited, several books [40, 41, 42, 24, 43] and papers [29, 44] review this area of research.

The previous work reported on yield optimization is primarily based upon the use of equivalent circuit models for active devices. This dependence ultimately limits present generation CAD since equivalent circuit models do not *predict* operation so much as compactly represent measurements on fabricated devices. Equivalent circuit elements do not naturally capture important nonlinearities and interrelationships of the physical entities they repre-

sent. Also, determining improved device design parameters from equivalent circuit elements is difficult because direct correspondence between physical parameters, equivalent circuit elements, and RF performance is not easily established.

In this work, a large-signal GaAs MESFET simulator for yield estimation and optimization is presented that does not rely on equivalent circuit techniques. The MESFET model in the simulator is based upon device physics with the advantage that a MIMIC can be simulated from process data all the way through to RF circuit performance. The integrated simulator allows a device design to be optimized based upon a desired RF performance specification. The small- and large-signal power amplifier performance measures developed in Section 3.1 are available for the yield pass-fall criterion. The yield optimizer's variables are physical parameters such as gate dimensions, channel donor distribution specifications, DC bias voltages, and material parameters. A standard Monte Carlo method is used to predict the process yield of a nominal MESFET design based upon a single performance measures' variation. The Monte Carlo yield estimate is then optimized using a quasi-Newton method. The quasi-Newton method is deterministic and is tolerant of the inherent noise in the yield estimate.

The resulting simulator has proved to be accurate under both class A and B operating conditions. Since simulations can be performed before fabrication, significant time, effort, and expense can be saved in the development of advanced MIMICs.

Small but uncontrollable disturbances in the fabrication process result in devices with geometries and doping profiles that deviate somewhat from nominal values. These variations in primary process parameters appear to be statistically simpler than the derivative variations of parameters for the corresponding equivalent circuit. For example, gate width and length are practically independent and both are uncorrelated with ion implant dose or energy. On the other hand, variations in equivalent circuit parameter values such as g_m, R_i, C_{gs}, C_{dg}, C_{ds}, and g_{ds} correlate significantly with each other [45, 46, 47]. Moreover, second order correlations (even large ones) may not suffice to characterize variations in equivalent circuit parameters [48].

Disturbances in physical parameters are easily characterized by a second order statistical model, a multivariate Gaussian. A multivariate Gaussian is specified by a mean vector and a covariance matrix. The mean vector is simply the nominal device design. The covariance matrix models the variances and covariances between physical parameters.

Given a Gaussian model for the parameter disturbance, the yield at some nominal design, x, is estimated by the following Monte Carlo algorithm:

1. Input mean or nominal design x,
2. Describe disturbances with multivariate probability function $p(v)$,
3. Draw a set of N disturbances v_i from $p(v)$, and
4. Approximate the yield as

$$Y(x) \approx \frac{1}{N} \sum_i \phi(x + v_i).$$

The disturbances v_i are generated as follows. Let C be the (positive definite) covariance of the parameters. Solve the eigenvalue problem $C = UWU^T$ for the matrix of eigenvectors U

and the diagonal matrix of (positive) eigenvalues W. From W construct the diagonal matrix w with entries that are the square roots of the entries of W. Then a vector z_i of independent, identically distributed Gaussian numbers of zero mean and unit variance is constructed by conventional techniques [19]. The uncorrelated disturbance vector z_i is converted to a fully correlated disturbance vector v_i with the formula $v_i = Uwz_i$.

The acceptance function ϕ is evaluated at each value of $x + v_i$ by comparing the performance measure under consideration with a user specified threshold. ($x + v_i$ is shown to have the correct statistics in Appendix B.) If the performance measure is greater than the threshold value, ϕ is set equal to one. Otherwise, ϕ is set equal to zero. The yield estimate is the then mean value of the acceptance function taken over the N samples.

In a Monte Carlo yield calculation, many devices are evaluated in the vicinity of a nominal design. In regions where the performance measure is relatively smooth, it is possible to use nearby points without incurring unacceptable estimation errors. The batch size of a Monte Carlo calculation sets a limit on expected precision which can be related to derivatives of performance measure to determine when it is appropriate to replace a numerically intensive performance measure calculation with a previously simulated result.

To reduce run times we have incorporated a simple data management system which maintains a binary tree database of previous simulations. When a new design is to be evaluated, the tree is searched for a similar design. If a similar design is close enough to the desired design, the stored performance measure is returned. Otherwise, the device model is called, and the simulation result is recorded in the tree.

This memory system will reduce the number of calls by varying amounts dependent upon the particular device design, the degree of nonlinearity, the number of disturbance parameters, and the extent of previous data. For the yield optimization results presented in Chapter 5, the number of calls was reduced by 16%.

Chapter 4

Mathematical Optimization Algorithm

This chapter is a chronological history of the TEFLON optimization group's work from June 1989 to June 1990. The optimization group's main goal was to assist other members of the TEFLON team with problems in optimization. The group also helped with other mathematical problems that the TEFLON team encountered.

4.1 Chronological Program Development

The first task for the optimization group was to obtain and test various optimization codes from the netlib. Two codes were obtained, LMDIF from Minpack and NL2SOL from TOMS. LMDIF, a least squares code, proved to be more portable and was more successful in solving the test problems we ran them on. LMDIF used the Levenberg-Marquardt algorithm with a forward difference approximation to the Jacobian.

During the summer and fall of 1989 TEFLON was obtaining poor values for some calculations, particularly near the end points of intervals. It was determined that part of the problem was due to the interpolator being used in TEFLON. We wrote a cubic piecewise Hermite polynomial interpolator to replace the existing interpolator. This interpolator uses a five-point algorithm to calculate the approximation to the derivatives at the interpolation points for the desired function. The interpolator was tested against several codes obtained from the netlib, and the existing interpolator in TEFLON, which was a code from IMSL. In all the problems tested our interpolator proved to be superior. In particular, it obtained much better values for the derivative of the functions to be interpolated near the end points of the interval.

In the spring of 1990 the group began working on device optimization. The goal in device optimization is to optimize a single device performance function such as input power, output power, or the gain, depending on from two to thirty parameters. These parameters include gate length, gate width, peak doping density in the channel, etc. These device configuration variables must fall within some specified bounds. So the problem becomes minimize $f : R^n \rightarrow R$, $f = f(x_1, \cdots, x_n)$ under the constraints that $l_i \leq x_i \leq \mu_i$, $i = 1, \cdots, n$.

Originally we were attempting to use least squares software to solve this problem. To use traditional least squares techniques we attempted to solve the problem, minimize (C-f) where $C > maxf$. $maxf$ is the maximum value obtained by the performance function f on the set of points that satisfy the above inequality constraints on the parameters. Unfortunately, the code the group was using (LMDIF, from Minpack) would not converge to a solution if C was greater than $maxf$ by more than a relatively small amount. Because $maxf$ varied widely as a function of the type and number of the parameters used, one needed to know the size of $maxf$ for the problem one was working on to a very close approximation. In general this was not the case. We felt that all least squares software would have this problem.

We next tried a quasi-Newton code for unconstrained optimization to work the device optimization problem. The code we tried used the BFGS approximation to the Hessian:

$$H_{k+1} = H_k + \frac{y_k y_k^T}{y_k^T s_k} - \frac{H_k s_k s_k^t H_k}{s_k^T H_k s_k}$$

where:

$$s_k = x_{k+1} - x_k$$

$$x_{k+1} = x_k + p_k$$

$$p_k = -H_k^{-1} \nabla f(x_k)$$

$$y_k = \nabla f(x_{k+1}) - \nabla f(x_k).$$

If the approximate Hessian is not positive definite, then $H_{k+1} = I$.

To take the constraints on the parameters into account, the algorithm took a large number of aggressive cutbacks in the line-search. Then, if the algorithm stepped outside of the hyperbox defined by the constraints, it was hoped that it would be able to quickly backtrack into the allowable area. However, when the code stepped outside of the hyperbox, numerical instability was encountered with the TEFLON software package.

We then tried working the problem using a projected gradient code. This code is a steepest descent code as long as the steps stay inside of the hyperbox defined by the constraints on the parameters. If the code steps outside of the hyperbox the step is the projection of the steepest descent step onto the surface of the hyperbox. The projection of the steepest descent step onto the hyperbox is accomplished by the following algorithm:

If $x_i^k - \beta^m \nabla f(x^k)_i \leq \ell_i$, then

$x_i^k = \ell_i$.

If $x_i^k - \beta^m \nabla f(x^k)_i \geq \mu_i$, then

$x_i^k = \mu_i$.

Otherwise

$x_i^{k+1} = x_i^k - \beta^m \nabla f(x^k)_i$.

Where:

1. x_i^k is the ith component of the kth point generated by the algorithm.
2. ℓ_i and μ_i are the lower and upper bounds on the ith parameter, respectively.
3. $\nabla f(x^k)_i$ is the ith component of the gradient of f at the kth point.
4. β is a user-supplied constant.
5. m is the first nonnegative integer such that
$$f(x^{k+1}) \leq f(x^k) + \sigma\beta^m \nabla f(x^k)^T (x^{k+1} - x^k)$$
is satisfied. σ is a user-defined constant.
6. f is scaled to be approximately unity.

Although this code was more successful then any code previously tried, it still became trapped in local minima. Thus, it was unable to obtain the global minima.

In an attempt to understand the noise in the problem, we tabulated values of the performance measure, small signal gain, for points on a rectangular grid covering the allowable parameter space for several pairs of parameters. The resulting tables indicated two levels of structure. The larger level was a single basin with its minimum lying somewhere within the hyperbox. The finer level of structure imposed a rough surface on the basin. This surface had many local minima. It was these local minima that were trapping the projected gradient algorithm.

In June 1990, the optimization group implemented the first version of the current code. This new implementation of the projected gradient algorithm used a monotonically decreasing sequence of steps for the finite difference approximation to the gradient. The initial step was taken to be half the length of the shortest side of the hyperbox. With this size of step the descent direction given by the approximate gradient was more affected by the global structure of the performance measure than by the local structure near the current iteration point. This way the algorithm was able to avoid the many local minima caused by the rough surface and move the iteration points toward one of the minima of the global structure.

A finite difference step size was rejected under two conditions:

1. If $\|\nabla f\|_\infty \leq tol$. Note that ∇f is the finite difference approximation to the gradient. tol is some estimate of the level of noise in the performance measure.

2. The backtracking line-search fails to find a point on the line segment between x^k and $x^k - \nabla f(x^k)$ that satisfies the Armijo condition.

If either of the above two conditions held, the finite difference step size was cut by two and the algorithm continued, starting from the last point generated by the algorithm with the previous finite difference step size. Decreasing the step size in this manner allowed the algorithm to work its way down into one of the basins of the global structure. The algorithm terminated when the step became so small that the finite difference gradient was only measuring changes in the rough surface. This algorithm proved successful in several test problems with similar structure to the device optimization problems we were currently working on. More conventional optimization techniques were unable to find the global minima of these test problems. The new algorithm was also tested on several device optimization problems

using the TEFLON software package. In each of these problems, the algorithm was started from a number of different initial points. Given a problem, the algorithm converged to the same global minimum from a variety of starting points. The algorithm was generally able to satisfy $\|\nabla f\|_\infty \leq tol$ at this point, for the finite difference step size not too small. The algorithm was tested against a simulate annealing code on two dimensional problems. Generally, the algorithm achieved larger values for the performance measure and it converged within far fewer function evaluations.

In July the single finite difference step was replaced with a vector of finite difference step sizes. Each element in this vector corresponded to one of the parameters in the problem. The initial finite difference step for each component of the gradient was set to half the length of the side of the hyperbox corresponding to that parameter. A vector of finite difference steps was rejected under the same conditions as a finite difference step in the first code. The vector of steps was then multiplied by 0.5 and the algorithm started again.

Three modifications were made to the code in the month of August.

- If $\|\nabla f\| < \|h_c\|$ set $\|\nabla f\| = \|h_c\|$. Where h_c is the current finite difference step size and $\|\cdot\|$ indicates the Euclidean norm. We tested this modification on two problems. The two problems used for the experiment both used small signal gain for the performance measure, and the following parameters:

  - Nmax, $1 \times 10^{16} \leq$ Nmax $\leq 1 \times 10^{18}$.
  - Range , $0.4 \leq$ Range ≤ 0.12.

  with the starting point $x_o = (\text{Nmax}, \text{Range}) = (9 \times 10^{17}, 0.10)$. However, the applied voltage was calculated differently in the two problems. The two methods were:

  - Method 1: ∇f unrestricted.
  - Method 2: $\|\nabla f\| \geq \|h\|$ where h is the vector of finite difference step sizes.

  The following table was obtained:

	method 1		method 2	
	PM	NFE	PM	NFE
A	1.282	66	1.409	63
B	1.879	33	1.879	24

  In the table PM stands for performance measure, and NFE stands for number of function evaluations. From the above table it appears that method 2 is superior. From plots of the surfaces of the problems defined above, the values obtained in the table were seen to be global maxima. In another problem not listed in the table method 2 was able to converge to a solution while method 1 was not.

- Default centered differences was replaced with default forward differences. Four experiments were run each with small signal gain as the performance measure. The experiments are summerized below:

Run	Parameters	Bounds	Starting Point
A	Gate length, Sigma	$[0.2, 1.0], [0.1, 0.2]$	$(0.9, 0.19)$
B	Sigma, Range	$[0.1, 0.2], [0.04, 0.12]$	$(0.19, 0.11)$
C	Nmax, Range	$[1 \times 10^{16}, 1 \times 10^{18}], [0.04, 0.12]$	$(9 \times 10^{17}, 0.10)$
D	Nmax, Gate Width	$[1 \times 10^{16}, 1 \times 10^{18}], [500.0, 2000.0]$	$(9 \times 10^{17}, 1000.0)$

The two methods used were:

- Method 1: ∇f obtained using forward differences.
- Method 2: ∇f obtained using centered differences.

The following table was obtained.

	method 1		method 2	
	PM	NFE	PM	NFE
A	31.31	60	31.06	53
B	14.43	58	14.68	88
C	14.09	63	14.10	74
D	15.81	62	17.13	76

In the table PM stands for performance measure, and NFE stands for number of function evaluations. From the above table it appears that using centered differences gives a more robust algorithm than using forward differences.

- The projected gradient step was replaced with a projected BFGS step. Three methods were tested against each other.
  - Method 1: Projected gradient.
  - Method 2: Projected BFGS, where the approximate Hessian is set to the identity every time a scale is rejected.
  - Method 3: Projected BFGS, where the approximate Hessian is updated throughout the run.

The Hessian was set to the identity whenever it was not positive definite in both projected BFGS methods. The two problems used were:

Run	Parameters	Bounds	Starting Point
A	Sigma, Range	$[0.1, 0.2], [0.04, 0.12]$	$(0.19, 0.11)$
B	Nmax, Range	$[1 \times 10^{16}, 1 \times 10^{18}], [0.04, 0.12]$	$(9 \times 10^{17}, 0.10)$

The following table summarizes the results.

	method 1		method 2		method 3	
	NFE	PM	NFE	PM	NFE	PM
A	88	14.68	81	14.63	55	12.22
B	63	14.09	65	13.41	63	14.15

The above table does not give conclusive evidence as to which is the best method. More experimentation is necessary.

During the fall of 1990 we began working problems of interest to other members of the TEFLON team. The first problem we worked was to maximize the gain for ITT 169 wafer MESFETs being operated in the class B mode. This was to be done by varying the channel doping profile. Several tests were run on models of the above mentioned devices. The code was able to increase the gain by 10% to 15% over the gain obtained by manually adjusting the parameters. However, in doing so the code drove the device model out of the class B mode and into the class A mode. The TEFLON source code was altered so that the user could specify what mode the model should operate in. With these changes in place, the code was able to increase the performance measure, maximum power-added efficiency (Max. PAE) depending on the three channel doping profile parameters nmax, range, and sigma, by 14% over a device obtained by manually adjusting the parameters. This improvement was obtained by using the parameters of the manually optimized device as a starting point.

However, when using other starting points the code found other local minima with impossibly large values of Max. PAE. After looking at a number of graphs of the performance measure on two dimensional subspaces of the parameter hyperbox, it was decided that the impossible performance measures were caused by impossibly large gate to source voltages. A penalty function was added to the performance measure that helped keep the algorithm out of regions of the hyperbox where these impossibly large gate to source voltages occurred.

At this time the group began working on several more problems:

1. Maximize maximum power-added efficiency for ITT 169 class B MESFETs by adjusting the matching circuit parameters: the real and imaginary parts of the load and generator impedances at the fundamental, second, and third harmonics.

2. Maximize small signal gain for ITT 169 MESFETs by adjusting the matching circuit parameters.

3. Maximize maximum power-added efficiency for ITT 169 class B MESFETs by adjusting the doping profile parameters and the matching circuit parameters.

The first problem was of particular interest at the time. The algorithm was able to obtain the same high performance measure (Max. PAE$\geq$ 80%) from many different starting places spread around the hyperbox. All of the final iteration points were within a few ohms of one another. The algorithm was able to obtain this high performance measure within several hundred function evaluations. This compared very favorably to the simulated annealing code also being used in TEFLON.

During the month of November several changes were made to the code for theoretical reasons. These changes were:

- Scaling - the hyperbox was mapped to the unit cube.

- After going through all scales the algorithm started over again at the first scale, continuing until no progress was made at any scale.

- The method for determining convergence at a particular scale was changed from $\|\nabla f\| \leq tol$ (where tol is an estimate of the noise in the performance measure) to $\|\nabla f\| \leq \frac{tol}{2h_c}$

The code with these three changes was never tested against the previous version of the code. These changes were made for theoretical reasons. However a slight improvement in the performance of the algorithm seemed to be obtained.

During the month of December various stopping criteria were tested. These criteria were equivalent to "convergence" at the current scale. All tests for convergence were made after the gradient at the current point was set to at least as large as the current scale. Four different criteria were tested:

- criteria 1: $\|\nabla f\| < \frac{tol}{2h_c}$, where h_c is the current finite difference step and tol is an estimate of the noise in the function.
- criteria 2: $\|\nabla f\| < 0.1h_c$.
- criteria 3: $\|x - (x - \nabla f)\hat{}\| < \frac{tol}{2h_c}$, where $\wedge$ indicates the projection onto the hyperbox.
- criteria 4: $\|x - (x - \nabla f)\hat{}\| < 0.1h_c$.

Six experiments were used for the tests. All of the experiments were done on a ITT 169 class A MESFET and had small signal gain as the performance measure. The following table summerizes these six problems.

Run	Parameters	Bounds	Starting Point
A	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(1.6 \times 10^{17}, 0.109)$
B	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(3.6 \times 10^{17}, 0.199)$
C	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(4.6 \times 10^{17}, 0.109)$
D	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(1.6 \times 10^{17}, 0.079)$
E	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(3.6 \times 10^{17}, 0.179)$
F	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(4.6 \times 10^{17}, 0.007)$

The results of these tests are summarized in the following table:

	criteria 1		criteria 2		criteria 3		criteria 4	
	NFE	PM	NFE	PM	NFE	PM	NFE	PM
A	77	13.171	77	13.171	77	13.171	77	13.171
B	76	13.206	98	13.207	76	13.206	98	13.207
C	61	13.204	82	13.208	61	13.204	82	13.208
D	72	13.139	88	13.140	72	13.139	93	13.140
E	71	13.140	110	13.140	71	13.140	142	13.140
F	54	12.006	DNC	DNC	44	12.006	DNC	DNC

DNC means the algorithm did not finish within ten minutes of CPU time.

As can be seen from the above table, rejecting the finite difference step size when

$$\|x - (x - \nabla f)\hat{}\| < \frac{tol}{2h_c}$$

appears to be the best method.

In January 1991 the code was modified further. Several changes were tried. The first was moving the check for convergence from after the gradient is extended to before the gradient is extended. The second was changing the projected gradient code to a projected SR1 code. The formula for calculating the SR1 approximation to the Hessian is given below:

$$S^{k+1} = S^k + \frac{r^k r^{k^T}}{r^{k^T} s^k}.$$

Where S^k is the previous SR1 approximation to the Hessian,

$$s^k = x^{k+1} - x^k$$

$$\text{and } r^k = y^k - S^k s^k \text{ where } y^k = \nabla f(x^{k+1}) - \nabla f(x^k).$$

The performance measure used in these experiments was small signal gain. Eight experiments were run. They are summarized in the following table:

Run	Problem	Bounds	Starting Point
A	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(1.6 \times 10^{17}, 0.079)$
B	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(2.6 \times 10^{17}, 0.179)$
C	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(4.6 \times 10^{17}, 0.007)$
D	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(1.6 \times 10^{17}, 0.109)$
E	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(3.6 \times 10^{17}, 0.199)$
F	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(4.6 \times 10^{17}, 0.109)$
G	Nmax, Sigma, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20], [0.05, 0.30]$	$(3.6 \times 10^{17}, 0.079, 0.199)$
H	Nmax, Sigma, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20], [0.05, 0.30]$	$(4.0 \times 10^{17}, 0.129, 0.210)$

The two methods used were:

- Method 1: projected gradient.
- Method 1: projected SR1.

The results of these experiments are summerized in the following table.

	method 1		method 2	
	PM	NFE	PM	NFE
A	13.139	72	13.140	66
B	13.140	71	13.140	71
C	12.006	44	12.006	44
D	13.171	77	13.207	75
E	13.206	76	13.205	75
F	13.204	61	13.204	56
G	13.781	97	13.810	86
H	12.873	218	13.004	188

In experiment C nether algorithm was able to move from the initial point. In experiment H the number of cutbacks was set to 10 instead of 4 as in the other experiments. As can be seen from the above table SR1 did as well or better on every problem.

During the month of March a cubic model of the performance measure in the quasi-Newton direction was added to the line-search. See section 6.3.2 of *Numerical Methods for Unconstrained Optimization and Nonlinear Equations*, by Dennis and Schnabel for details of the implementation. This model is used to calculate the optimum value for the cutback factor. One deviation was made from the implementation as given by Dennis and Schnabel. The line-search was terminated after 10 cutbacks and not when the size of the reduced step became less than some specified value. This method of doing the line-search was compared to the linear cutback strategy of using cutbacks of $\frac{1}{2}$ that was currently being used in the algorithm. The performance measure used in these experiments was small signal gain. Eight experiments were run. They are summarized in the following table:

Run	Problem	Bounds	Starting Point
A	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(1.6 \times 10^{17}, 0.079)$
B	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(2.6 \times 10^{17}, 0.179)$
C	Nmax, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.001, 0.20]$	$(4.6 \times 10^{17}, 0.007)$
D	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(1.6 \times 10^{17}, 0.109)$
E	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(3.6 \times 10^{17}, 0.199)$
F	Nmax, Sigma	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30]$	$(4.6 \times 10^{17}, 0.109)$
G	Nmax, Sigma, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30], [0.001, 0.20]$	$(3.0 \times 10^{17}, 0.080, 0.080)$
H	Nmax, Sigma, Range	$[1 \times 10^{17}, 6 \times 10^{17}], [0.05, 0.30], [0.001, 0.20]$	$(3.0 \times 10^{17}, 0.200, 0.01)$

In experiments C, G, and H the minimum scale was set to 0.00005 and the number of cutbacks used was 10. In the remaining experiments the minimum scale was set to 0.005, and the number of cutbacks used was 4. In all cases the scaling factor for the performance measure was $\frac{1}{20}$. The two methods are listed as:

- Method 1: Projected SR1 with cubic line-search.
- Method 2: Projected SR1 with linear line-search.

The results of these experiments are summerized in the following table.

	method 1		method 2	
	PM	NFE	PM	NFE
A	13.138	59	13.140	66
B	13.140	80	13.140	71
C	13.140	235	13.140	259
D	13.207	62	13.207	75
E	13.207	73	13.205	75
F	13.207	59	13.204	56
G	13.107	201	13.170	246
H	13.327	293	13.327	316

As can be seen from the above table the cubic model performed better in 6 out of the 8 experiments. It also did better in every case where a large number of function evaluations were done. Because of these results the cubic model will be the line-search procedure used from now on.

In April the group assisted the engineers in the TEFLON group with applying the algorithm to their work. This involved looking at the output from runs on their problems and

advising them how to set the various parameters, such as the scaling factor for the performance measure, the minimal size for the finite difference steps and the number of cutbacks to be used in the line-search. This work was useful not only because it helped the engineers accomplish their work, but it also gave us insights into the performance of the code.

We also began working on the theoretical aspects of the algorithm. This work involved analyzing the behavior of projected gradient algorithms in the presence of noise in the performance measure and when analytical derivatives are not available. We feel that this work will give insight into the workings of the algorithm. In particular it is hoped that this analysis will give insight into when to terminate the iteration, and on rates of convergence.

4.2 Current Algorithm

A description of the current algorithm is as follows:

1. Given

$$x^c,\ h,\ S^c,$$

calculate

$$f(x^c),\ \nabla f(x^c),\ \text{and}\ y = (x^c - \nabla f(x^c))^\wedge.$$

If

$$\|x^c - y\| \leq \frac{minscal}{2h}$$

set

$$h = 0.5h,\ \text{and}\ S^c = I$$

then return to 1. $(V)^\wedge$ indicates the projection of V onto the hyperbox, and *minscal* is the minimal scale used. *minscal* is an estimate of the minimum distance between points in the hyperbox for which an appreciable difference in the value of the performance measure can be detected and S^c is the SR1 matrix.

2. Otherwise update S^c using the SR1 update described earlier in this report. Determine if S^c is positive definite. If it is not, set $S^c = I$. In our code positive definiteness of the matrix is checked in the Linpack code DCHDC, a double precision Cholesky decomposition routine. Setting $S^c = I$ if the approximate Hessian is not positive definite guarantees that the step is always a descent direction.

3. Solve

$$S^c p = \nabla f(x^c).$$

If

$$\|p\|_2 \leq h$$

then set

$$p = \frac{h}{\|p\|_2} p.$$

The matrix equation is solved by use of the Linpack subroutines DCHDC and DPOSL. First DCHDC does a Cholesky decomposition on the matrix and then DPOSL solves the factored system.

4. Calculate the cutback factor α for the step. The algorithm for calculating α will be discussed latter in this report. below for details. If

$$\|\alpha p\| < h,$$

set

$$h = 0.5h, \text{ and } S^c = I$$

then return to 1.

5. Calculate

$$x^+ = (x^c - \alpha p)\wedge.$$

If

$$f(x^+) \leq f(x^c) - 10^{-4}\alpha \nabla f^T p,$$

then set

$$x^c = x^+$$

and return to 1. Otherwise return to 4.

The algorithm for calculating the cutback factor for the line-search goes as follows:

If no previous cutbacks for this p have been made, set $\alpha = 1$. If

$$x_i^+ = u_i \text{ and } x_i^c \neq u_i \text{ or } x_i^+ = l_i \text{ and } x_i^c \neq l_i$$

for any i set

$$\alpha = 0.5\hat{\alpha}.$$

Where $\hat{\alpha}$ is the previous cutback factor that was used to calculate x^+. If $\hat{\alpha}$ is the first cutback factor for this p such that

$$x_i^+ \neq u_i \text{ if } x_i^c \neq u_i, \text{ and } x_i^+ \neq l_i \text{ if } x_i^c \neq l_i$$

for every i, then α should be the unique minimizer of

$$(f(x^c - \hat{\alpha}p) - f(x^c) - \hat{\alpha}\nabla f(x^c)^T p)\alpha^2 + \hat{\alpha}\nabla f(x^c)^T p\alpha + f(x^c).$$

Otherwise, α is the local minimizer to

$$a\alpha^3 + b\alpha^2 + \nabla f(x^c)^T p\alpha + f(x^c).$$

Where:

$$\begin{bmatrix} a \\ b \end{bmatrix} = \frac{1}{\hat{\alpha} - \dot{\hat{\alpha}}} \begin{bmatrix} \frac{1}{\hat{\alpha}^2} & \frac{-1}{\dot{\hat{\alpha}}^2} \\ \frac{-\dot{\hat{\alpha}}}{\hat{\alpha}^2} & \frac{\hat{\alpha}}{\dot{\hat{\alpha}}^2} \end{bmatrix} \begin{bmatrix} f(x^c - \hat{\alpha}p) - f(x^c) - \nabla f(x^c)^T p\hat{\alpha} \\ f(x^c - \dot{\hat{\alpha}}p) - f(x^c) - \nabla f(x^c)^T p\dot{\hat{\alpha}} \end{bmatrix}.$$

In the above matrix equation, $\dot{\hat{\alpha}}$ is the cutback factor previous to $\hat{\alpha}$. The local minimizer to this cubic polynomial is

$$\alpha = \frac{-b + \sqrt{b^2 - 3a\nabla f(x^c)^T p}}{3a}.$$

The code as described above has been successful in solving a number of problems of interest to the TEFLON team. These problems include:

- Device optimization: modifying the physical parameters of the device so as to obtain maximum performance for a given performance measure.
- Yield optimization: centering the design of a device within the hyperbox defined by the physical parameters to obtain the greatest number of manufactured devices that perform above a given threshold for a given performance measure.
- Parameter extraction: modifying the physical parameters so as to match the performance of a given given device for a given set of performance measures.

Chapter 5

Yield Optimization Experiments

The simulator was used to conduct a series of yield optimization experiments. Three types of MESFET devices were selected: an ion implanted device, a buried channel device, and a uniform channel device. The ion implanted MESFET design was based upon a commercial device that had been empirically optimized by a standard procedure for maximum power-added efficiency. The device is capable of good RF performance and, as will be shown, the simulator was not able to alter the design to obtain significant design improvements for PAE. The buried channel MESFET design was also based upon an industrial device, but the device in this case was a prototype and was not optimum. The simulator significantly modified the original design to improve performance. The starting design for the uniform channel MESFET was determined using standard, first principle design techniques. The initial design proved not to be optimum and was also significantly modified by the simulator to obtain improved performance. Starting from these MESFET designs, we then sought to optimize the yield of each device structure relative to to small-signal transducer gain, output power at 1 dB gain compression, and maximum power-added efficiency. All devices were embedded in a 50 Ω circuit so that performance variations based upon device design, rather than circuit tuning conditions, could be investigated.

The experiments were conducted by specifying the experiment variables and estimating the disturbance covariance matrices. We selected the variables by performing sensitivity analyses on each device structure. The results of these analyses are given in Appendices C, D, and E. The variables to which the performance measures are most sensitive were included. For all the device types, the performance measures were most sensitive to the variables which specify the gate geometry, the channel donor distribution, and the DC bias. The variables for each device type are listed in Table 5.1. For these experiments the gate length is perturbed about the nominal manufacturable value which held fixed and is not subject to optimization. Previous experience indicates that the optimizer always drives gate length to its minimum permitted value.

We assumed that each device's variables are statistically independent. The covariance matrices are therefore diagonal. The diagonal elements are the squares of estimated standard deviations for each variable. In all cases, except the gate width, the standard deviations are taken to be 3% to 10% of the nominal values for initial designs. The gate width standard deviation is estimated to be the gate length standard deviation times the number of gate fingers. The variances are listed in Table 5.1.

Ion Implanted Device	
Variable	Variance
L_g	$1.6\times10^{-3}\ (\mu m)^2$
W_g	$4.0\times10^{-2}\ (\mu m)^2$
E	$5.6\times10^{1}\ (keV)^2$
D	$1.4\times10^{22}\ \left(\frac{ions}{cm^2}\right)^2$
V_{GG}	$1.0\times10^{-2}\ (V)^2$
V_{DD}	$9.0\times10^{-2}\ (V)^2$

Buried Channel Device	
Variable	Variance
L_g	$1.6\times10^{-3}\ (\mu m)^2$
W_g	$2.6\times10^{-2}\ (\mu m)^2$
t_{low}	$1.7\times10^{-6}\ (\mu m)^2$
t_{high}	$5.3\times10^{-6}\ (\mu m)^2$
N_{low}	$5.6\times10^{31}\ \left(\frac{ions}{cm^3}\right)^2$
N_{high}	$1.6\times10^{33}\ \left(\frac{ions}{cm^3}\right)^2$
V_{GG}	$2.5\times10^{-3}\ (V)^2$
V_{DD}	$9.0\times10^{-2}\ (V)^2$

Uniform Channel Device	
Variable	Variance
L_g	$1.6\times10^{-3}\ (\mu m)^2$
W_g	$4.0\times10^{-2}\ (\mu m)^2$
t_{chnl}	$2.3\times10^{-4}\ (\mu m)^2$
N_{chnl}	$2.5\times10^{31}\ \left(\frac{ions}{cm^3}\right)^2$
V_{GG}	$2.5\times10^{-3}\ (V)^2$
V_{DD}	$9.0\times10^{-2}\ (V)^2$

Table 5.1: Disturbance covariance matrices for ion implanted device, buried channel device, and uniform device

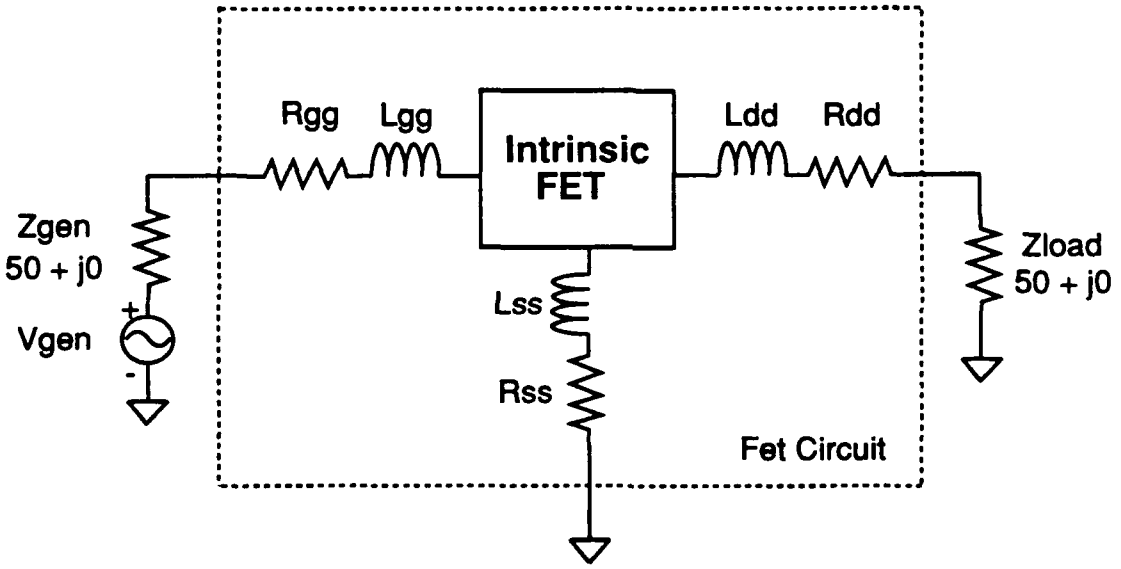
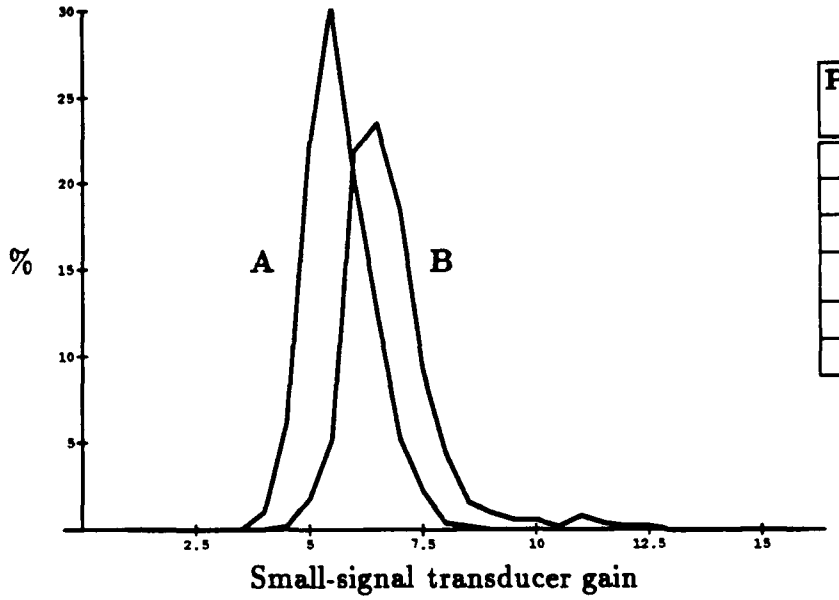


Figure 5.1: The circuit simulated during yield optimizations.

A number of other conditions were specified for the experiments. Three harmonics were used during harmonic balance calculations. The simulated circuit was reduced as shown in Figure 5.1. The impedances presented to the gate and drain of the MESFET, as previously indicated, were 50 + j0 Ω at all harmonics. During each yield optimization, the number of sample devices for each yield estimate was 100. The number of sample devices in the presented yield histograms is 500.

In Figures 5.2, 5.3, and 5.4 we show the initial and optimized yield histograms for ion implanted, buried channel, and uniform channel devices when small-signal transducer gain is used as the acceptance criterion. The three initial designs all have similar initial gain distributions with means varying from 5.1 to 5.9 while the standard deviations range from 0.7 to 1.1. The buried channel device exhibits the best improvement with a distribution mean increasing to 16.0. All the optimized distributions exhibit greater spread than their



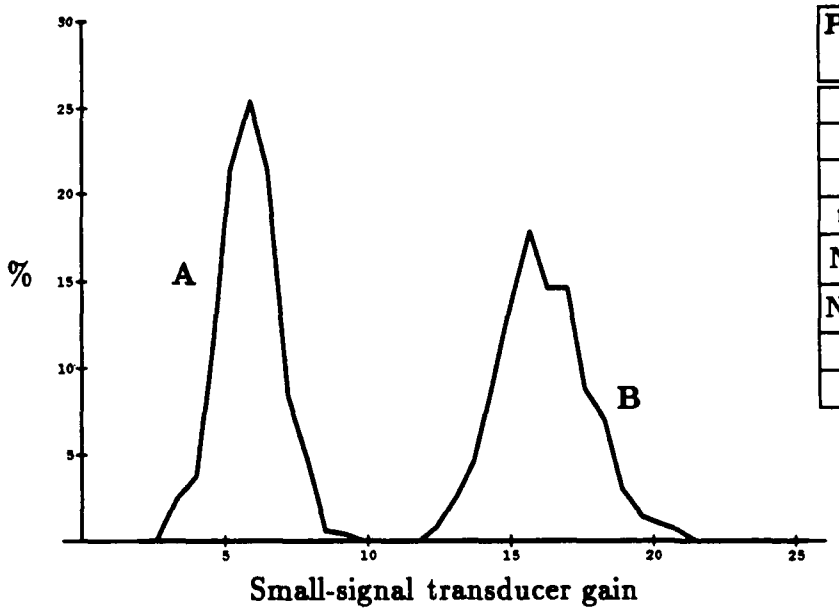
Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	609
E (keV)	150	133
D $\left(\frac{ions}{cm^2}\right)$	4.0×10^{12}	3.7×10^{12}
V_{GG} (V)	-2.0	-2.1
V_{DD} (V)	6.0	6.2

Figure 5.2: Simulated histograms of ion implanted device optimized for yield relative to small-signal transducer gain. **A** – initial design. **B** – optimized design.

corresponding initial distributions. The standard deviations of the optimized designs range from 1.4 to 2.3. The increased spread results from the optimized designs being in a region were the gain is more sensitive to perturbations in the design parameters. For all three devices the optimizer changes the gate width the most. These changes improve the matching between the transistor and the 50 Ω circuit. This large change in gate width would not necessarily be expected for a tuned circuit. The buried and uniform channel devices also exhibit large changes in their biases. For both devices, V_{GG} and V_{DD} increase. This bias shift is to a region of higher transconductance. The increased transconductance improves the small-signal gain.

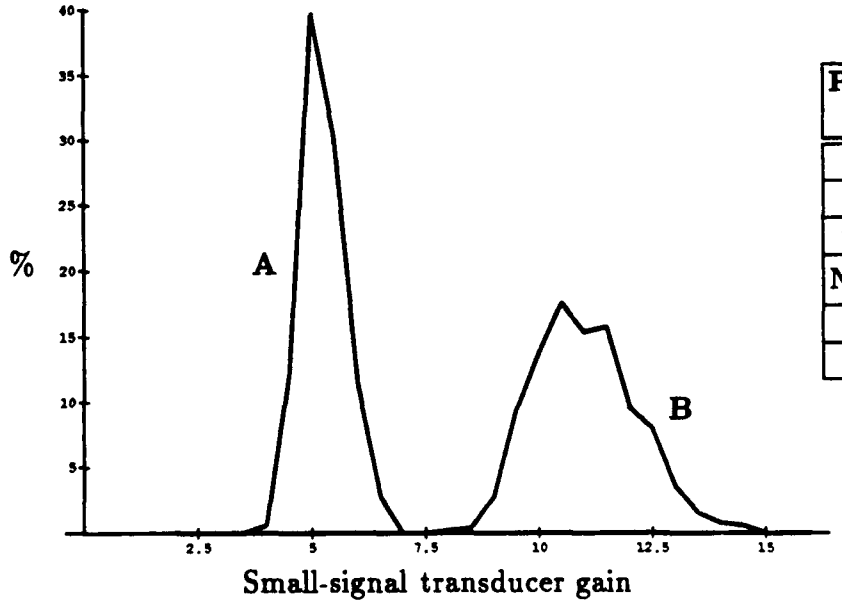
Figures 5.5, 5.6, and 5.7 show the initial and optimized yield histograms for ion implanted, buried channel, and uniform channel devices when output power at 1 dB gain compression is used as the acceptance criterion. The initial designs again have similar performance. The initial design distribution means range from 253 to 316 mW while the standard deviations vary from 55 to 71 mW. The uniform channel device shows the greatest increase in distribution mean to 2283 mW. However, the distribution spread is more than twice that of the two other optimized designs. In all three cases, the optimized designs show marked improvement over the initial designs. Again, the optimizer changes the gate widths of all three devices the most. However in this case, the increased gate widths allow more current to flow through the devices — impedance matching becomes a secondary consideration. For the buried and uniform channel devices V_{GG} and V_{DD} increase considerably. V_{DD} is also markedly increased for the ion implanted device. The biases change, along with the channel doping and gate width, so as to maximize the intersection of the 50 Ω load line and the device I-V curves.

Yield optimization using maximum power-added efficiency as the acceptance criterion was also performed. Figures 5.8, 5.9, and 5.10 show the initial and optimized yield histograms for ion implanted, buried channel, and uniform channel devices. The initial designs in this case are not all similar. The initial uniform channel design has a distribution mean



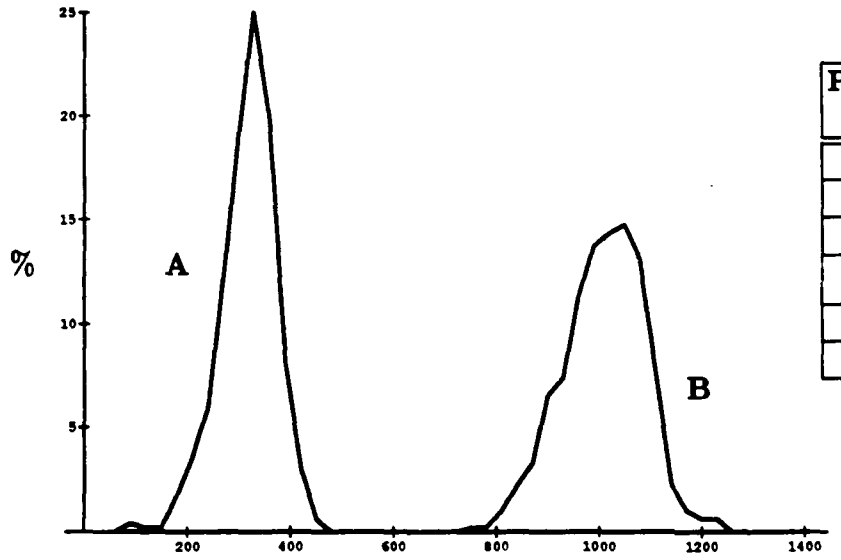
Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	800	401
t_{low} (μm)	0.026	0.026
t_{high} (μm)	0.046	0.062
N_{low} $\left(\frac{ions}{cm^3}\right)$	1.5×10^{17}	1.2×10^{17}
N_{high} $\left(\frac{ions}{cm^3}\right)$	8.0×10^{17}	7.9×10^{17}
V_{GG} (V)	-1.0	-0.13
V_{DD} (V)	6.0	7.5

Figure 5.3: Simulated histograms of buried channel device optimized for yield relative to small-signal transducer gain. A – initial design. B – optimized design.



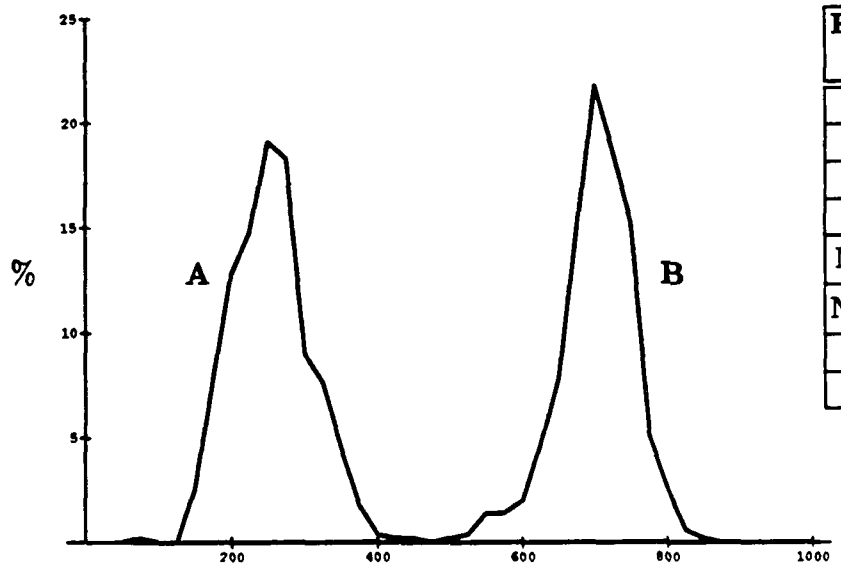
Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	400
t_{chnl} (μm)	0.30	0.22
N_{chnl} $\left(\frac{ions}{cm^3}\right)$	1.0×10^{17}	9.0×10^{16}
V_{GG} (V)	-1.0	-0.29
V_{DD} (V)	6.0	12.3

Figure 5.4: Simulated histograms of uniform channel device optimized for yield relative to small-signal transducer gain. A – initial design. B – optimized design.



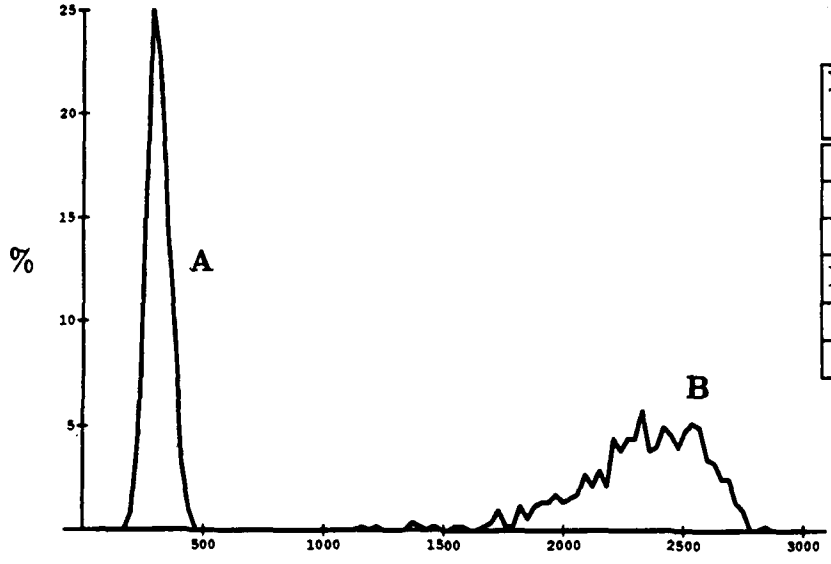
Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	2755
E (keV)	150	171
D $\left(\frac{\text{ions}}{\text{cm}^2}\right)$	4.0×10^{12}	3.3×10^{12}
V_{GG} (V)	-2.0	-2.0
V_{DD} (V)	6.0	9.6

Figure 5.5: Simulated histograms of ion implanted device optimized for yield relative to output power at 1 dB gain compression. **A** – initial design. **B** – optimized design.



Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	800	2298
t_{low} (μm)	0.026	0.026
t_{high} (μm)	0.046	0.049
N_{low} $\left(\frac{\text{ions}}{\text{cm}^3}\right)$	1.5×10^{17}	1.4×10^{17}
N_{high} $\left(\frac{\text{ions}}{\text{cm}^3}\right)$	8.0×10^{17}	7.8×10^{17}
V_{GG} (V)	-1.0	-0.65
V_{DD} (V)	6.0	10.0

Figure 5.6: Simulated histograms of buried channel device optimized for yield relative to output power at 1 dB gain compression. **A** – initial design. **B** – optimized design.

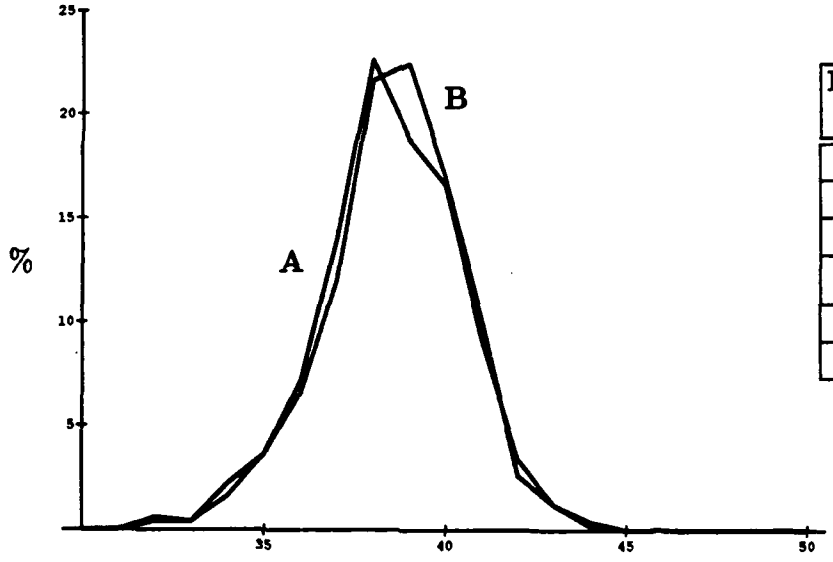


Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	2952
t_{chnl} (μm)	0.30	0.22
N_{chnl} $\left(\frac{ions}{cm^3}\right)$	1.0×10^{17}	7.3×10^{16}
V_{GG} (V)	-1.0	-0.44
V_{DD} (V)	6.0	16.0

Figure 5.7: Simulated histograms of uniform channel device optimized for yield relative to output power at 1 dB gain compression. **A** – initial design. **B** – optimized design.

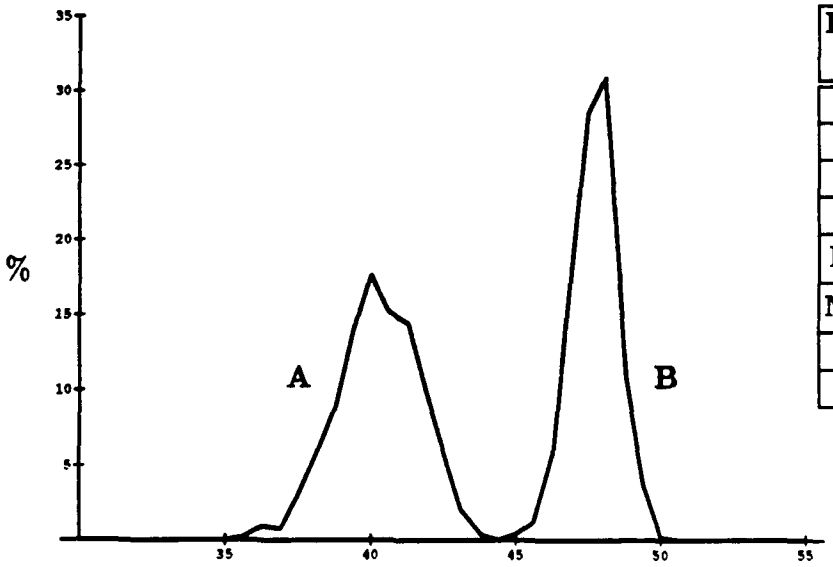
of 19%, whereas, the initial ion implanted and buried channel designs have distribution means of 38.5% and 40.0%, respectively. Yield optimization improved the uniform channel design's distribution mean to 40.9%, but the optimized buried channel design has the best performance with a distribution mean of 47.6%. We note no improvement in the ion implanted design. This result was anticipated since the ion implanted initial design is based on a mature industry device which has been empirically optimized for maximum power-added efficiency. As was the case with the gain and output power at 1 dB gain compression, the largest changes occur in the gate width and the DC bias. The changes in gate width improve the match to the 50 Ω circuit. The bias point shift in such a way as to minimize the DC power supplied to the device while maximizing the intersection of the 50 Ω load line and the device I-V curves.

Different optimum device designs result for each of the specified performance criteria. That is, an optimum PAE design is different from an optimum design for either maximum output power or gain. This series of experiments indicates that the buried channel device is the best device structure of the three when gain and power-added efficiency are of primary concern. The uniform channel device gave the best average performance for output power at 1 dB gain compression, but the performance distribution exhibits excessive variance. These result, of course, only apply to the devices embedded in a 50 Ω circuit. Different results are possible when circuit tuning conditions are considered.



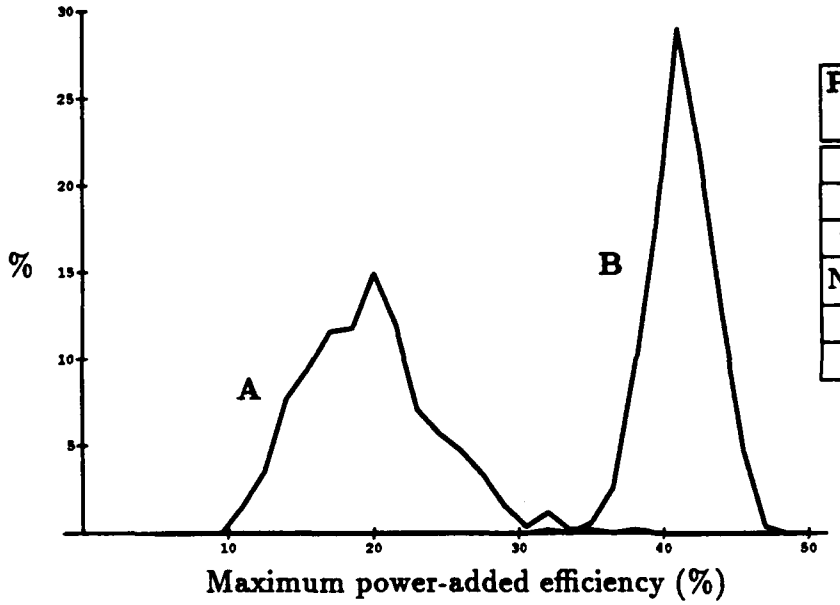
Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	814
E (keV)	150	159
D $\left(\frac{ions}{cm^2}\right)$	4.0×10^{12}	4.1×10^{12}
V_{GG} (V)	-2.0	-2.2
V_{DD} (V)	6.0	5.7

Figure 5.8: Simulated histograms of ion implanted device optimized for yield relative to maximum power-added efficiency. **A** – initial design. **B** – optimized design.



Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	800	380
t_{low} (μm)	0.026	0.027
t_{high} (μm)	0.046	0.044
N_{low} $\left(\frac{ions}{cm^3}\right)$	1.5×10^{17}	1.3×10^{17}
N_{high} $\left(\frac{ions}{cm^3}\right)$	8.0×10^{17}	7.8×10^{17}
V_{GG} (V)	-1.0	-0.43
V_{DD} (V)	6.0	5.8

Figure 5.9: Simulated histograms of buried channel device optimized for yield relative to maximum power-added efficiency. **A** – initial design. **B** – optimized design.



Parameter	Design	
	A	B
L_g (μm)	0.40	0.40
W_g (μm)	1000	1210
t_{chnl} (μm)	0.30	0.25
N_{chnl} $\left(\frac{ions}{cm^3}\right)$	1.0×10^{17}	9.1×10^{16}
V_{GG} (V)	-1.0	-2.2
V_{DD} (V)	6.0	6.7

Figure 5.10: Simulated histograms of uniform channel device optimized for yield relative to maximum power-added efficiency. **A** – initial design. **B** – optimized design.

Chapter 6

Conclusions

The NCSU large-signal, non-linear MESFET simulator (TEFLON) has been significantly advanced and enhanced with RF sensitivity, yield determination, and yield optimization routines. The physics based device simulator allows, for the first time, determination of DC and RF performance directly in terms of structural, doping, bias, and RF circuit tuning conditions. Doping profiles can be determined theoretically using the Stanford SUPREM 3.5 process simulator, or experimentally using a physical parameter extraction routine that has been developed. The simulator (TEFLON) has been structured to link directly with SUPREM, which must be obtained directly from Stanford. The physical parameter extraction routine is included in TEFLON.

The yield simulator uses a Monte Carlo method that makes numerous calls to the device model, until an accurate estimate of the yield is obtained. Incorporation of an advanced near-global optimization algorithm permits the initial device design and operating conditions to be varied until a maximized yield is obtained. In this manner 'design centering' can be efficiently performed. The mathematical optimizer is a quasi-Newton method which uses decreasing gradient scales to overcome the estimator's Monte Carlo noise. The optimizer permits physical parameters to be adjusted until a maximized yield in any specified RF performance measure is obtained. Typically, linear gain, RF output power at 1 dB gain compression, and maximum power-added efficiency are used as the performance measure.

Use of the simulator for yield determination and design centering is demonstrated. It is interesting that this investigation reveals that the same design is not optimum for the different performance measures. In fact, if optimized performance with maximum yield is to be obtained, each application will require a specialized device and circuit design.

The simulator has been verified to be quantitatively accurate for simulation of MESFETs operating at C and X-bands. Verification tests were performed using device data supplied by ITT, Raytheon, Texas Instruments, General Electric and Hughes. Excellent agreement between simulated and measured data was obtained.

An early version of the simulator and User's Manual was offered and supplied at no cost to any MIMIC Program participants that desired a copy. Copies were delivered to ITT, Raytheon, Texas Instruments, Hughes, TRW, Martin-Marietta, Compact Software, General Electric, Wright-Patterson AFB, and Fort Monmouth. In addition, user training was provided to ITT and Raytheon, also at no cost. Effective use of the simulator requires some learning, but the effort should be productive. The updated version of the complete

simulator (TEFLON 5.0) and updated User's Manual are available from NCSU.

The simulator is state-of-the-art and represents a significant advancement in the development of microwave computer-aided design tools. When used by a skilled engineer in industrial applications, the simulator should prove useful in efforts to reduce the time and costs required to produce advanced MIMICs.

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Appendix A

Yield Estimate Error

The true yield is

$$\overline{\phi} = \langle \phi(x_i) \rangle, \forall x_i.$$

The estimate Y has the correct mean

$$\langle Y \rangle = \frac{1}{N} \sum_i \langle \phi(x_i) \rangle = \frac{1}{N} \sum_i \overline{\phi} = \overline{\phi}$$

and so is an *unbiased* estimate of $\overline{\phi}$. The variance of Y is

$$var(Y) = \langle (Y - \langle Y \rangle)^2 \rangle$$

is equal to

$$var(Y) = \frac{1}{N^2} \sum_j \sum_i \langle (\phi(x_i) - \overline{\phi}) \, (\phi(x_j) - \overline{\phi}) \rangle.$$

But the disturbances of different devices are uncorrelated so that

$$var(Y) = \frac{1}{N^2} \sum_j \sum_i \delta_{i,j} \langle (\phi(x_i) - \overline{\phi})^2 \rangle = \frac{var(\phi)}{N}$$

since $\delta_{i,j}$ is the usual Kronecker delta which is unity when $i = j$ and is zero otherwise. Now

$$var(\phi) = \langle (\phi(x) - \overline{\phi})^2 \rangle = \langle \phi^2 \rangle - \overline{\phi}^2$$

but $\phi(x)$ is either unity or zero so that $\phi(x_i)^2 = \phi(x_i)$ and so

$$\langle \phi(x)^2 \rangle = \langle \phi(x) \rangle = \overline{\phi}$$

and therefore, combining these results

$$var(Y) = \frac{1}{N} var(\phi) \simeq \frac{1}{N} (Y - Y^2) = \frac{Y(1 - Y)}{N}.$$

Appendix B

Statistics of Disturbance Vector Sequences

We now show that our Gaussian generator produces disturbance vector sequences with the correct statistics. Let $y = x + v$, then the mean of y is x.

$$\langle y \rangle = \langle x \rangle_z + Uw\langle z \rangle_z$$

because the expectation operator $\langle . \rangle$ is linear. But x is constant so that $\langle x \rangle_z = x$. By construction, the random vector z is zero mean so that $\langle z \rangle_z = 0$.

Also, the covariance of y is C:

$$\mathrm{cov(y)} = \langle (\mathrm{y} - \langle \mathrm{y} \rangle_z)\ (\mathrm{y} - \langle \mathrm{y} \rangle_z)^{\mathrm{T}} \rangle_z$$

which is

$$\mathrm{cov(y)} = \langle (\mathrm{Uwz})\ (\mathrm{Uwz})^{\mathrm{T}} \rangle_z = \langle \mathrm{Uwzz^{T}w^{T}U^{T}} \rangle_z.$$

But U and w are constant with respect to the expectation operator and $\langle zz^T \rangle_z = I$ the identity matrix since z is a vector of independently distributed, (Gaussian) random variables of zero mean and unit variance, so

$$\mathrm{cov(y)} = \mathrm{Uw}\langle \mathrm{zz^{T}} \rangle_z \mathrm{w^{T}U^{T}} = \mathrm{Uww^{T}U^{T}}.$$

Finally w is the diagonal matrix of the square roots of W, so that $ww^T = W$ and

$$\mathrm{cov(y)} = \mathrm{UWU^{T}},$$

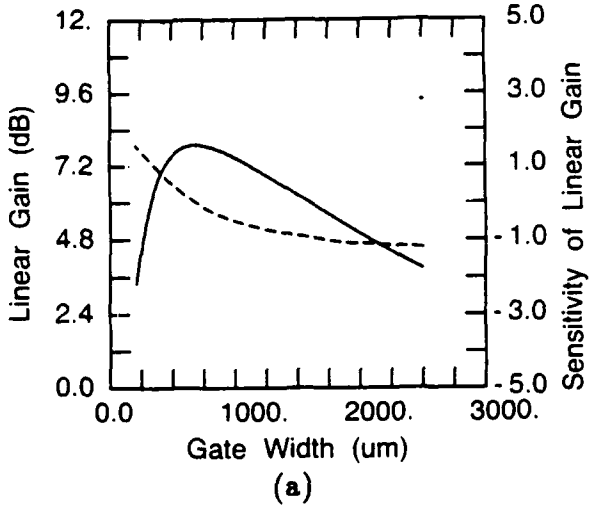
which is simply the originally specified covariance C, since U and W were obtained by solving the eigenproblem problem $C = UWU^T$.

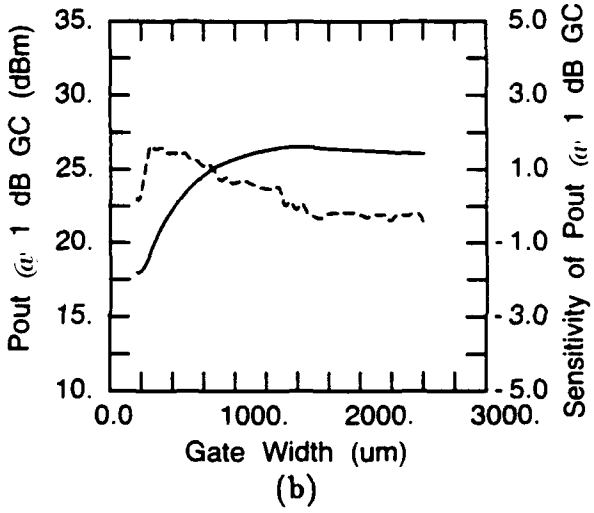
Therefore the formula $y = x + Uwz$ converts a vector of zero-mean, unit-variance independently random numbers into a vector of process disturbances that agree with the specified mean and covariance of those disturbances.

Appendix C

Sensitivity Analysis of Ion Implanted Device

The data presented in this Appendix is an sensitivity analysis of an ion implanted MESFET device. The study was undertaken to identify the parameters to which certain performance measures are most sensitive. The performance measures considered were the small-signal transducer gain, the output power at 1 dB transducer gain compression, and the maximum transducer power-added efficiency. These measures are most sensitive to gate length, gate width, implant dose, implant energy, gate-source bias voltage, and drain-source bias voltage. During the simulations for which the DC bias voltages were not analysis parameters, the gate-source bias voltage was set to $0.5V_{po}$, and the drain-source bias voltage was set to $0.5V_{dsbd}$.





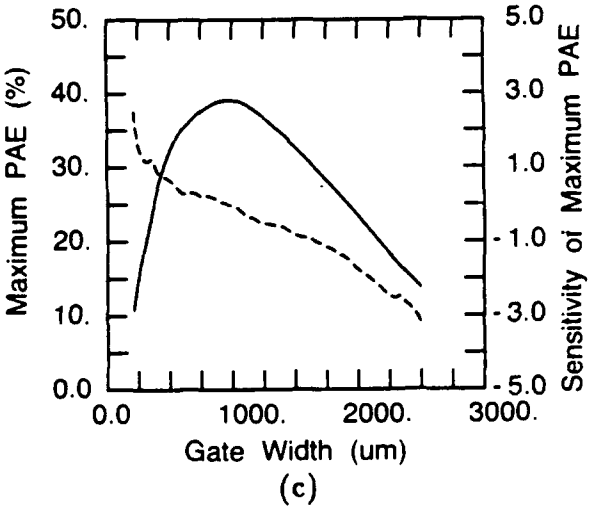
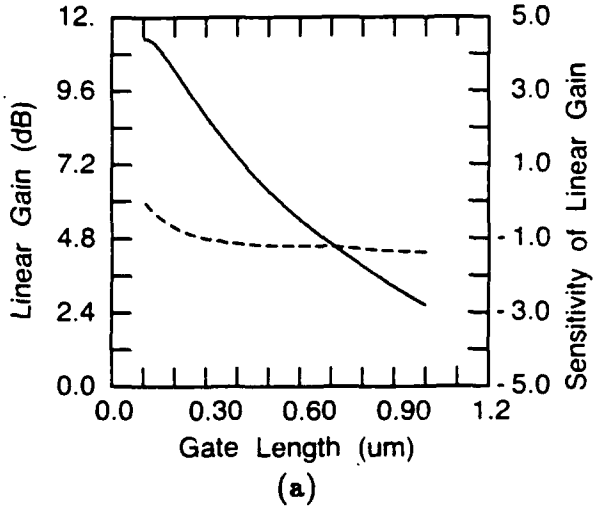
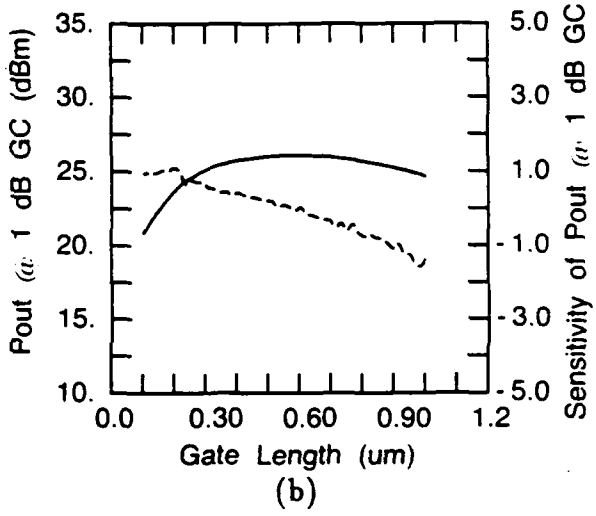


Figure C.1: The effect of gate width variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





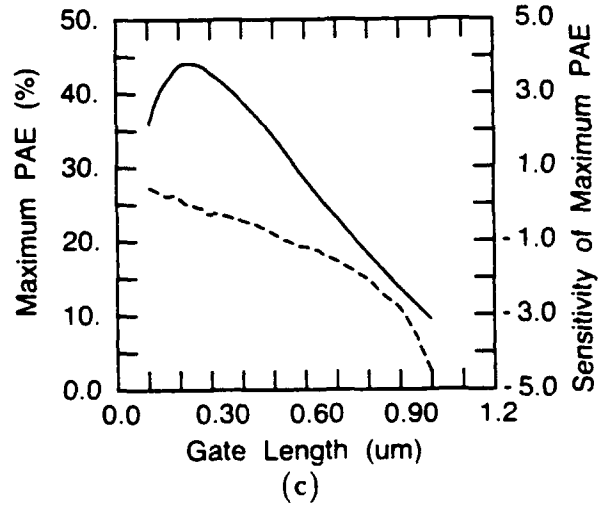
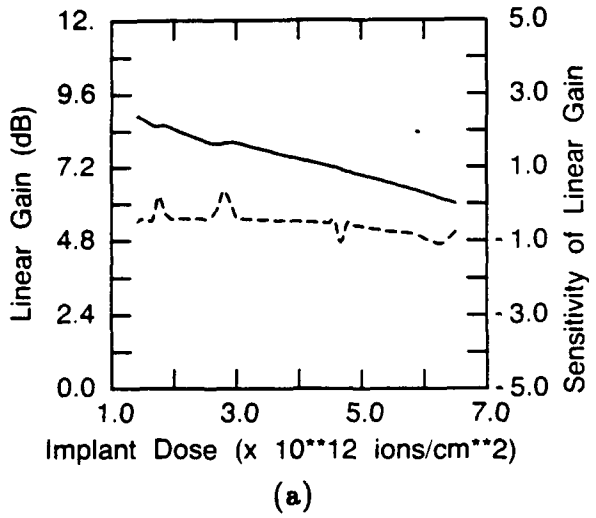
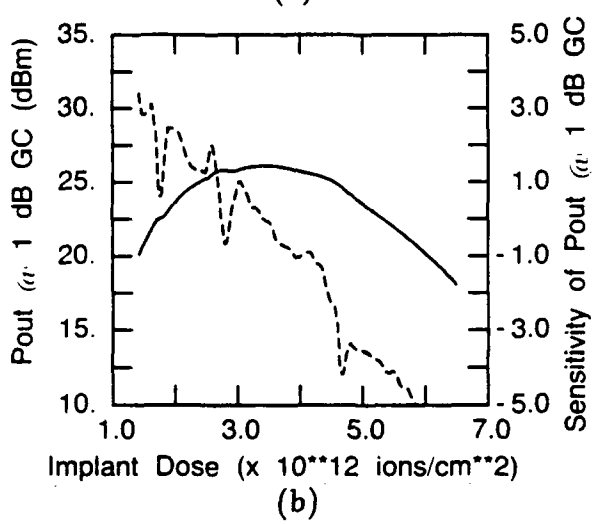


Figure C.2: The effect of gate length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





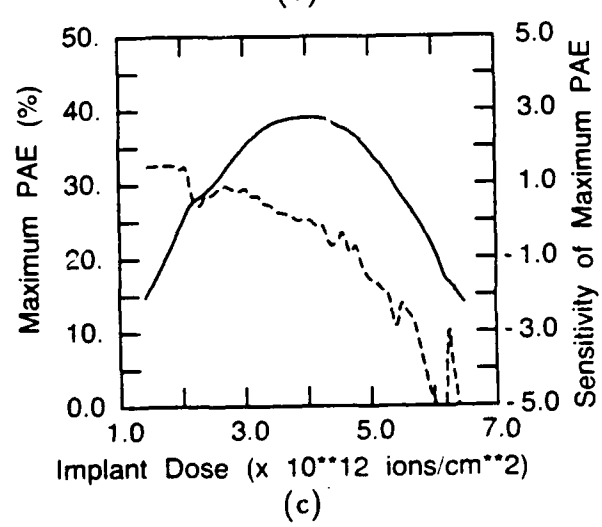
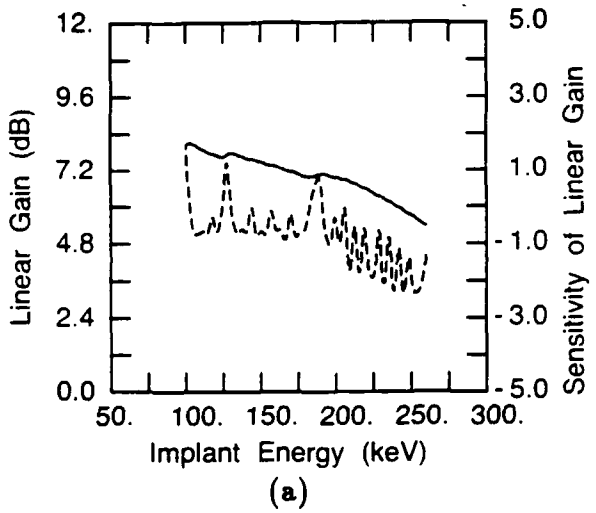
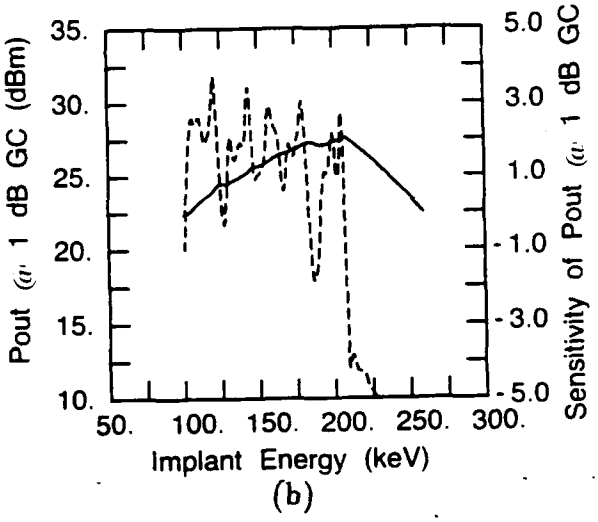


Figure C.3: The effect of implant dose variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





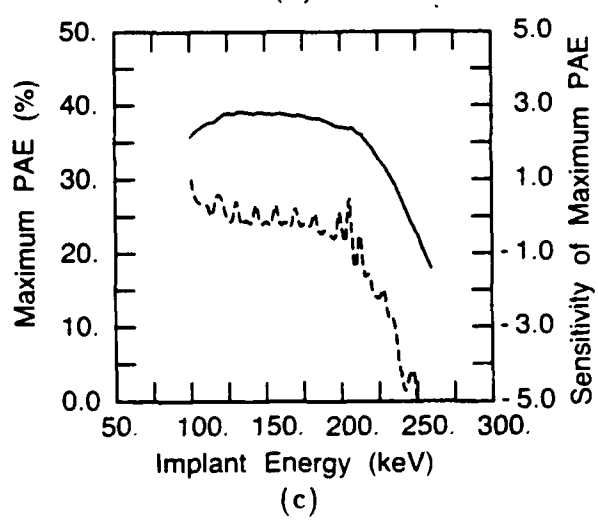
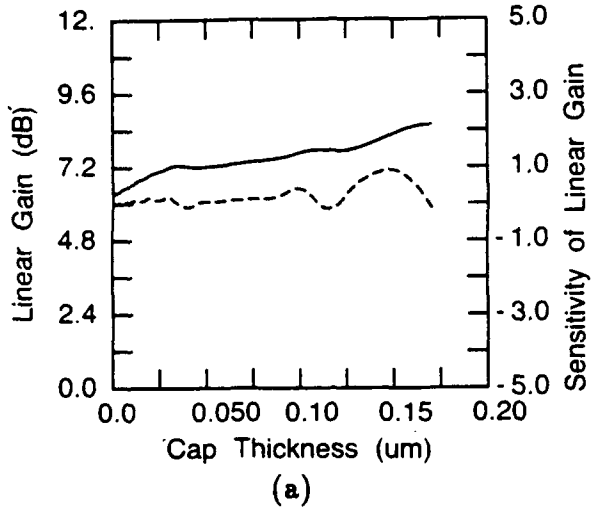
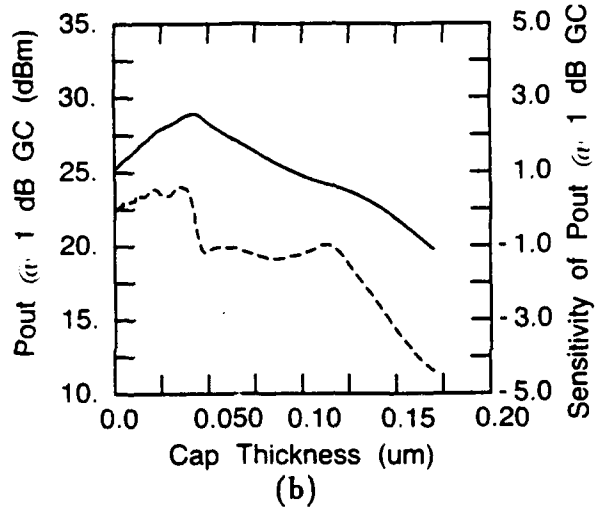


Figure C.4: The effect of implant energy variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





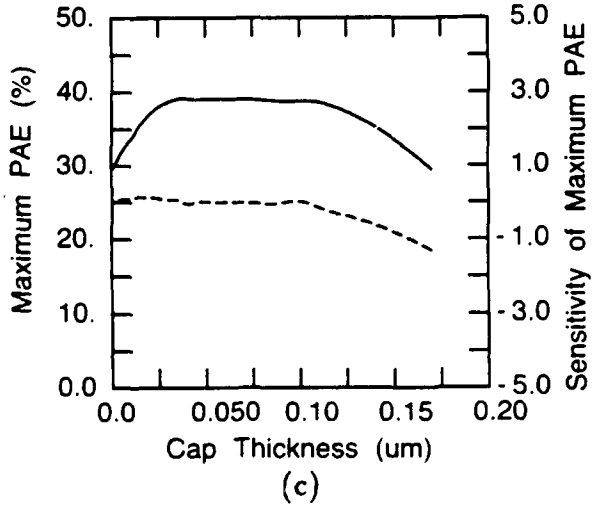
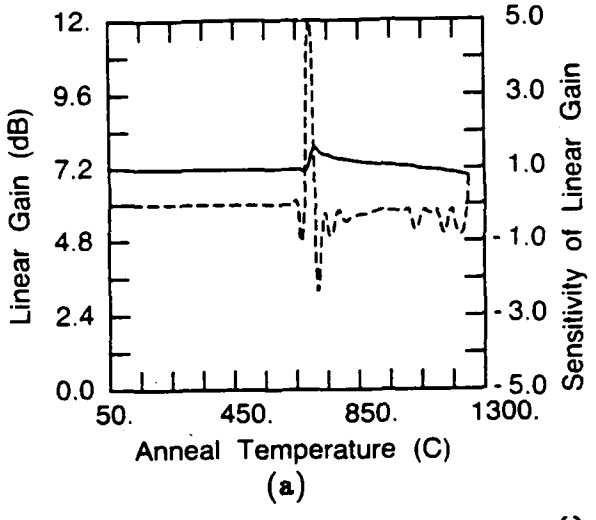
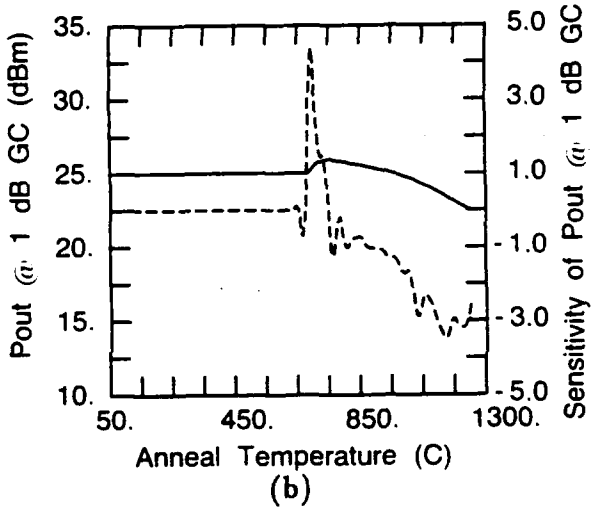


Figure C.5: The effect of implant cap thickness variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





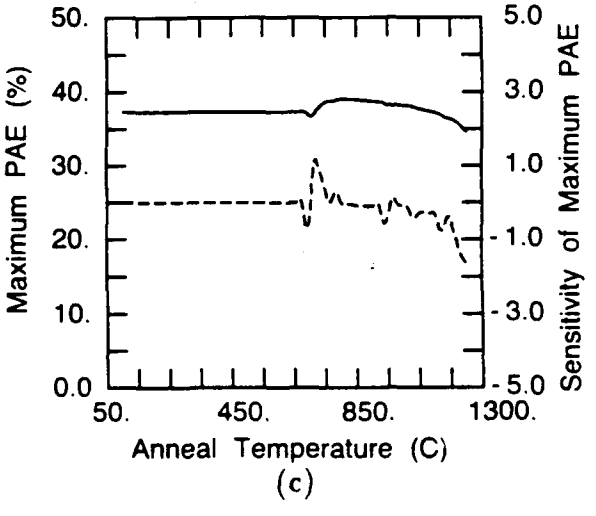
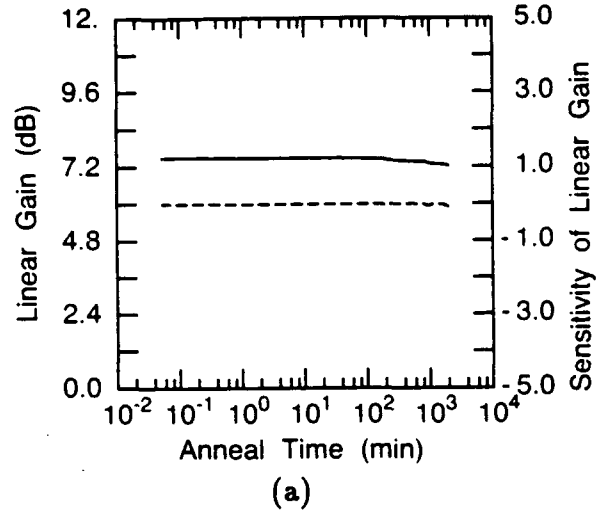
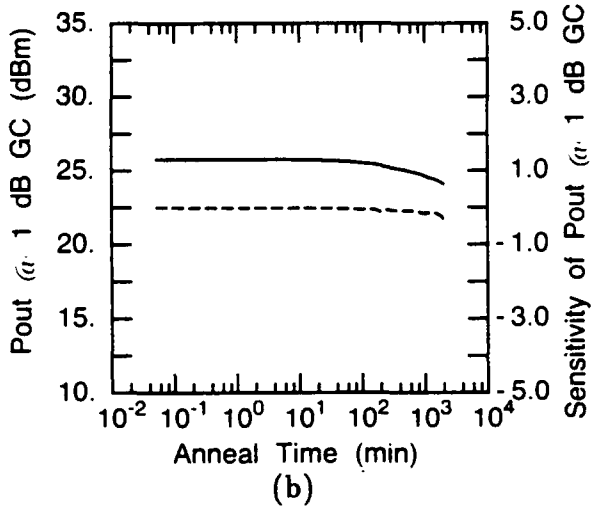


Figure C.6: The effect of implant anneal temperature variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





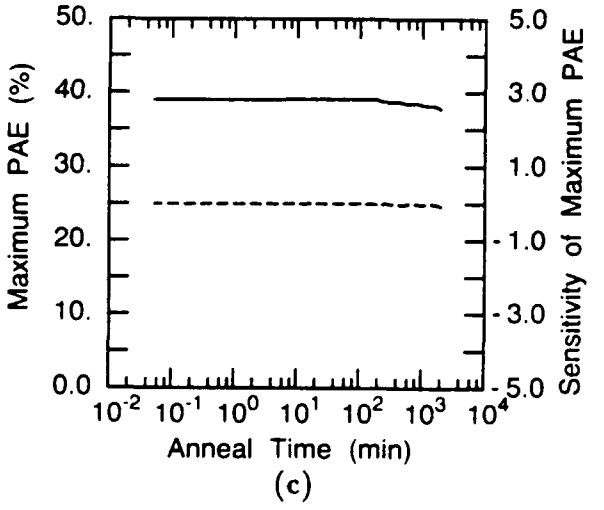
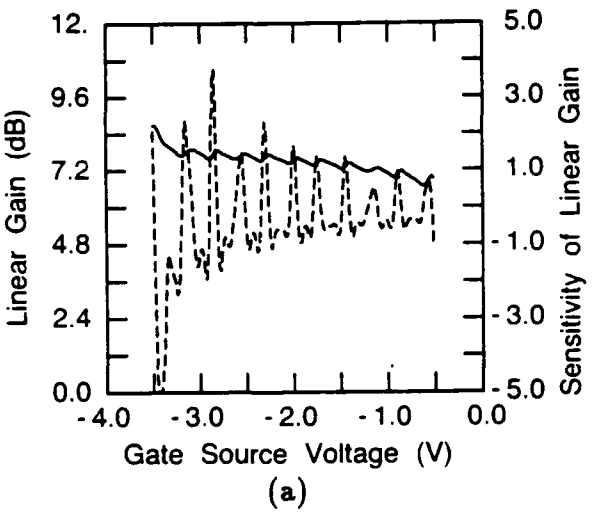
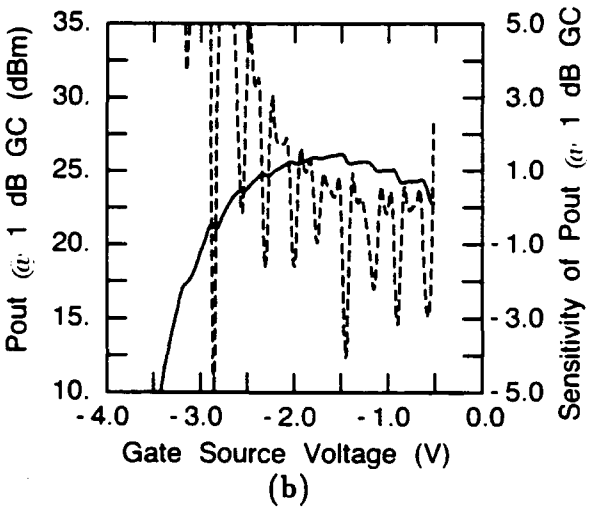


Figure C.7: The effect of implant anneal time variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





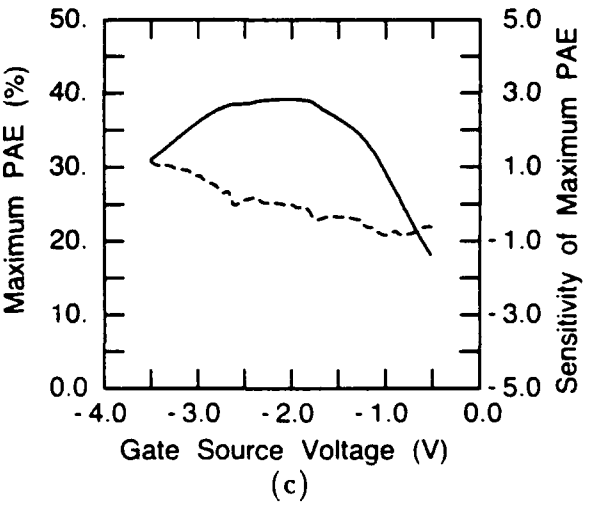
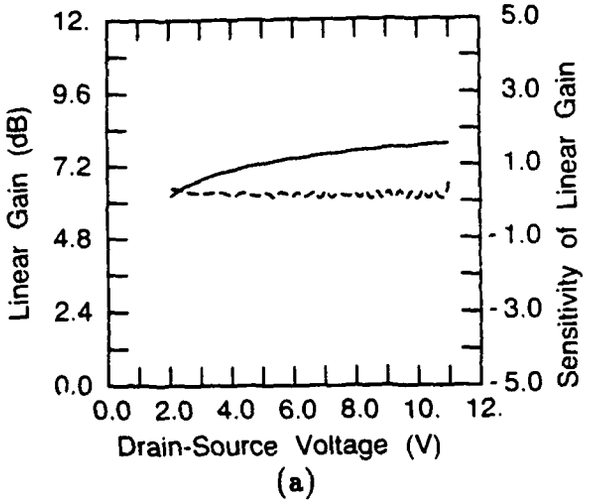
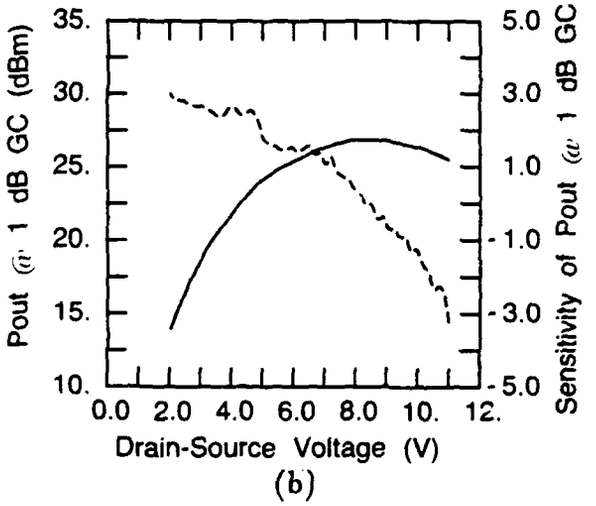


Figure C.8: The effect of DC gate-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





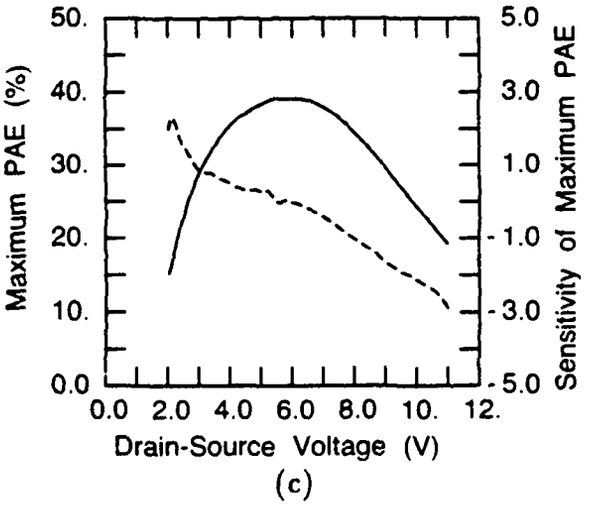
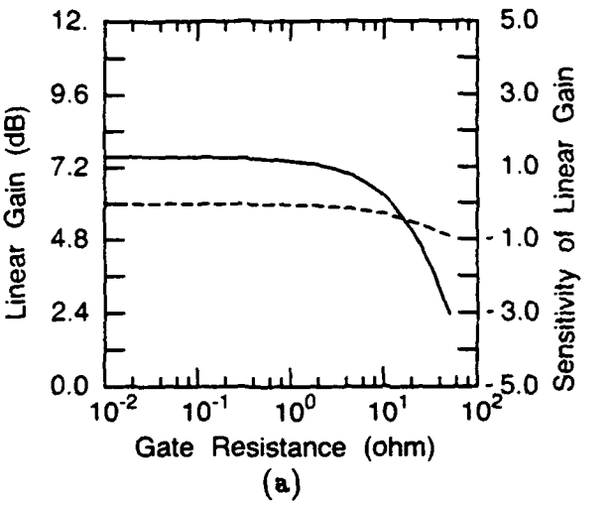
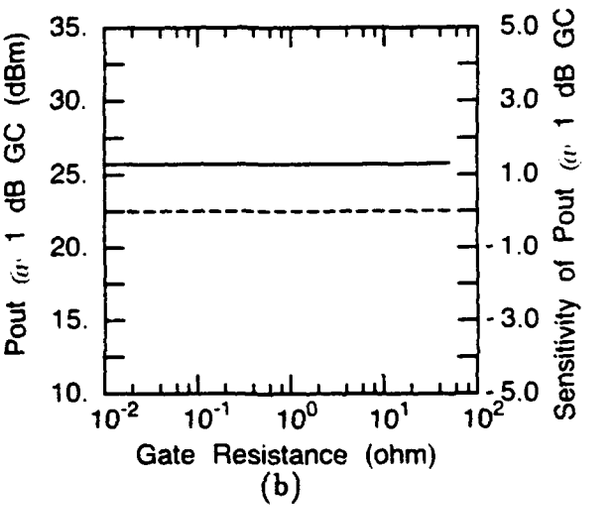


Figure C.9: The effect of DC drain-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





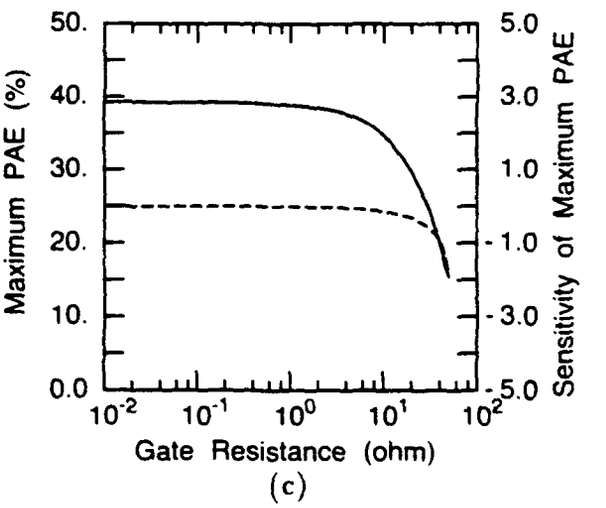
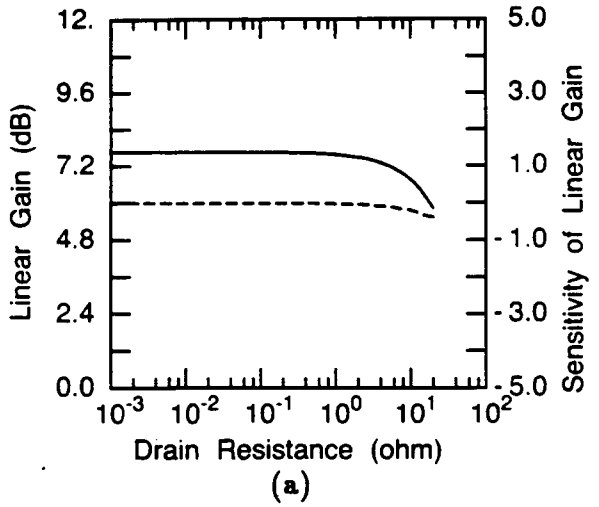
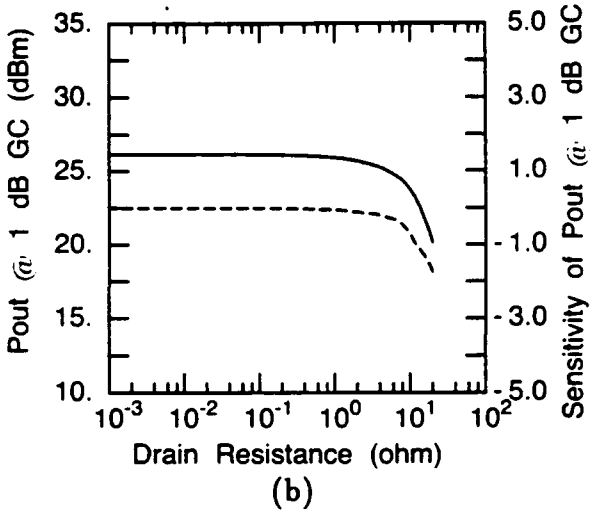


Figure C.10: The effect of parasitic gate resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





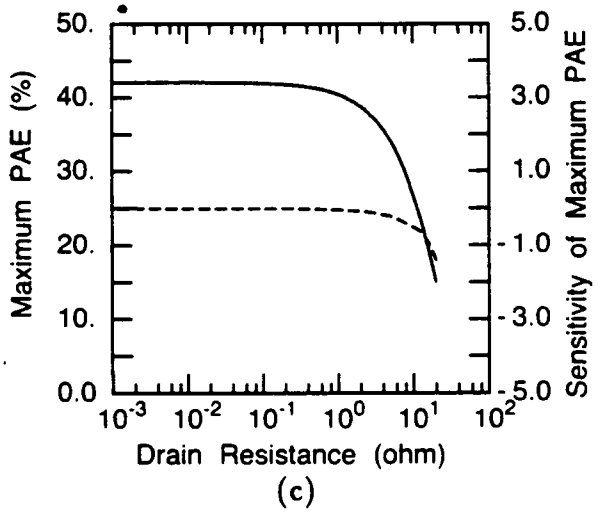
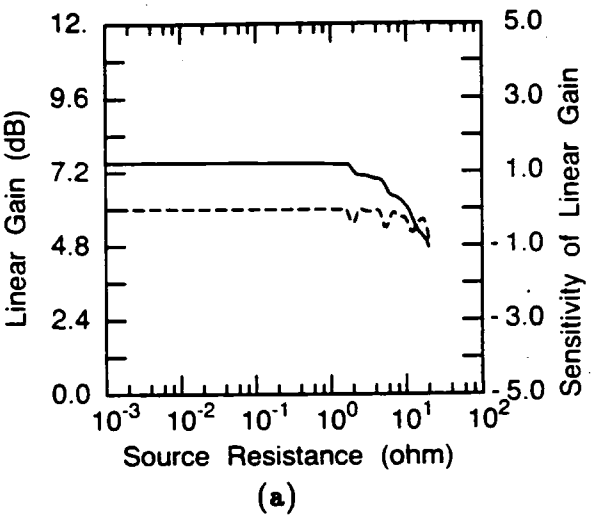
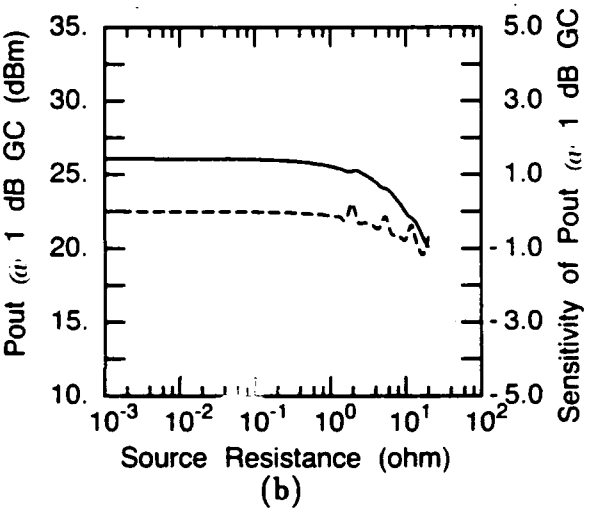


Figure C.11: The effect of parasitic drain resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





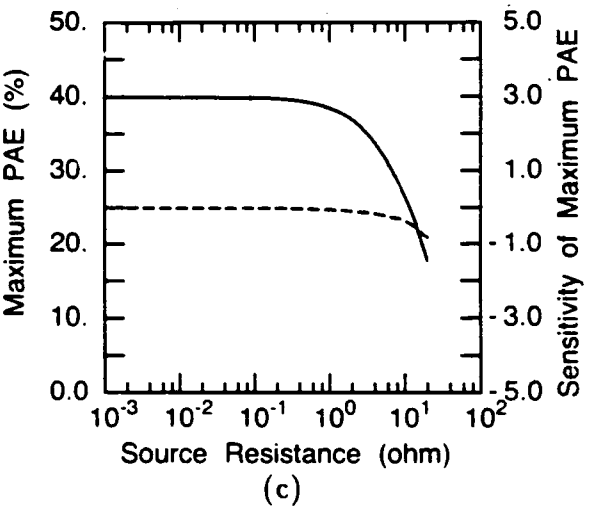
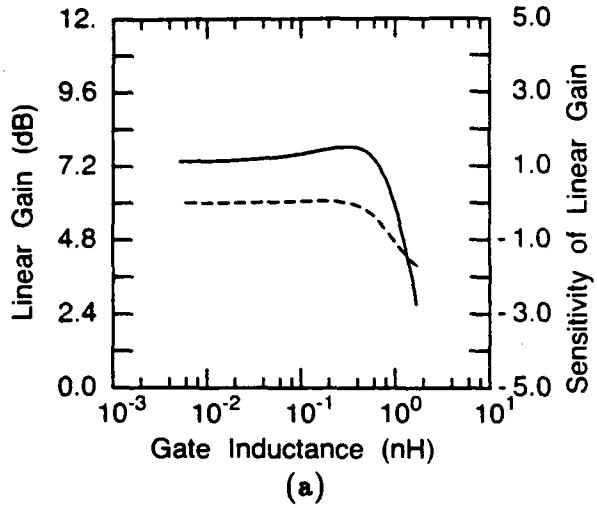
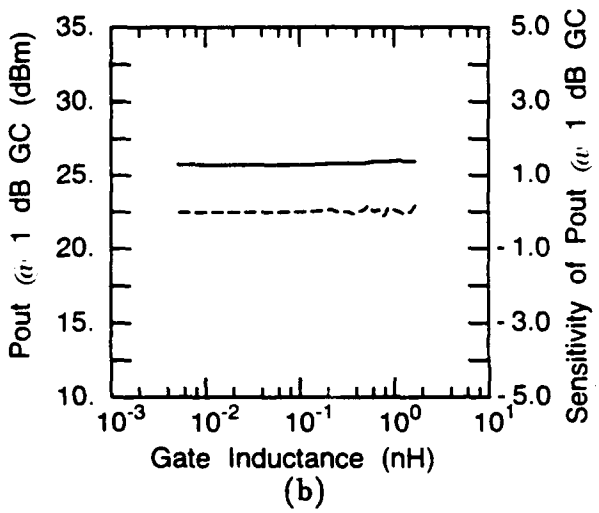


Figure C.12: The effect of parasitic source resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





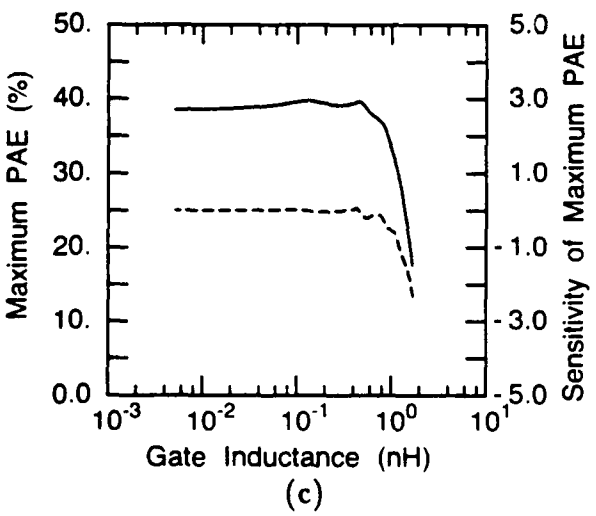
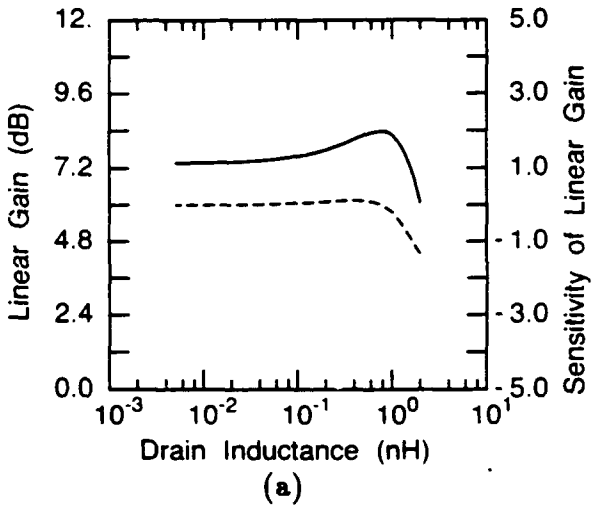
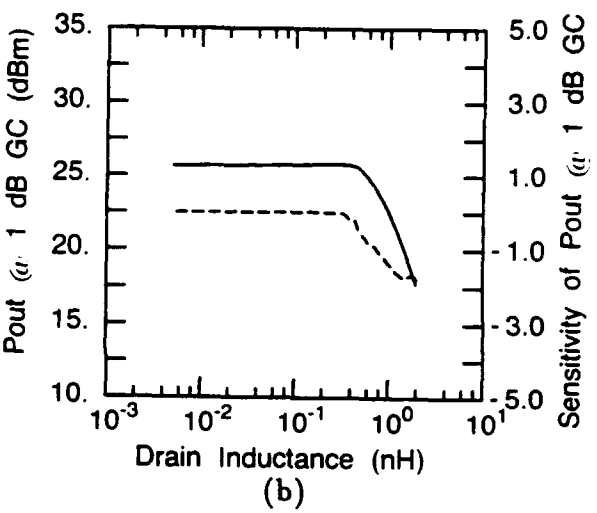


Figure C.13: The effect of parasitic gate inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





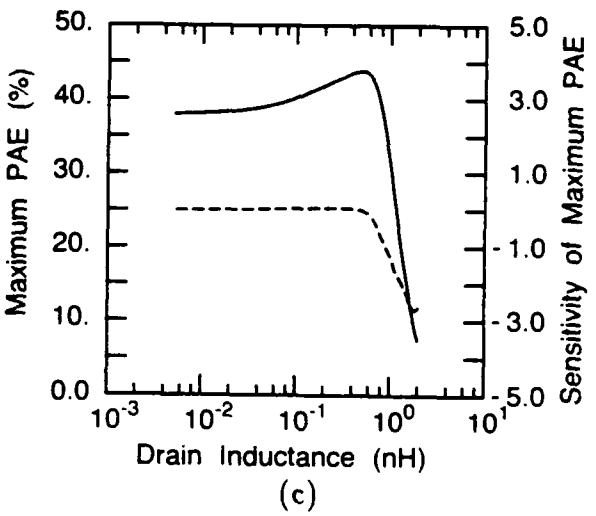
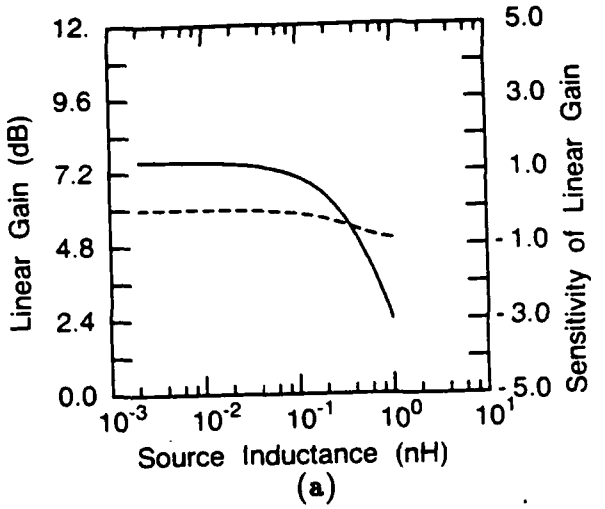
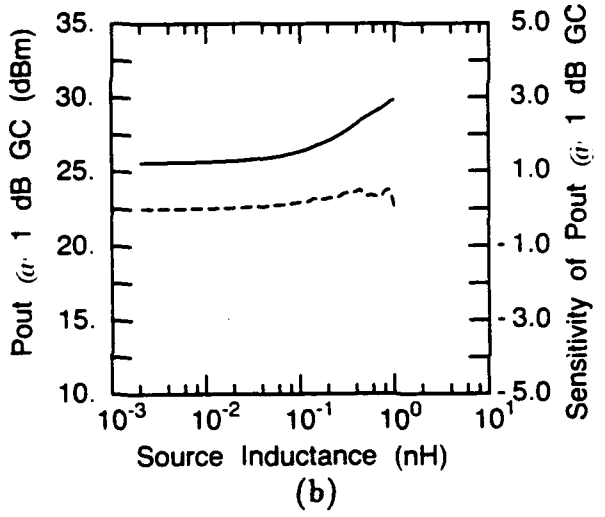


Figure C.14: The effect of parasitic drain inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





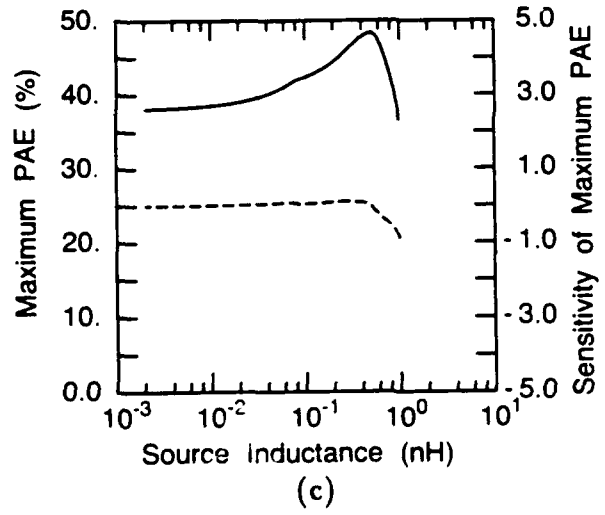
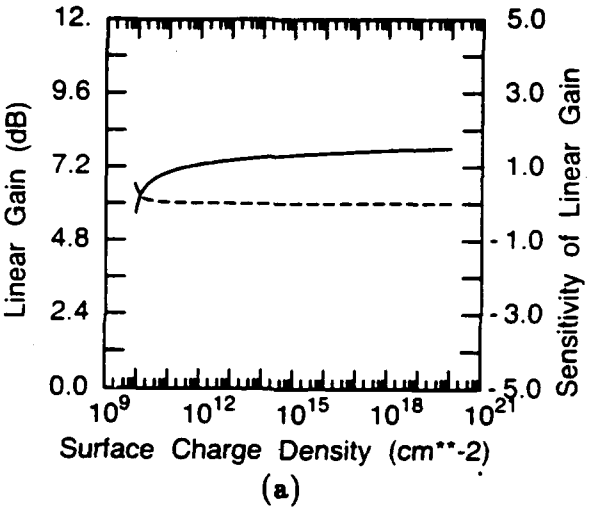
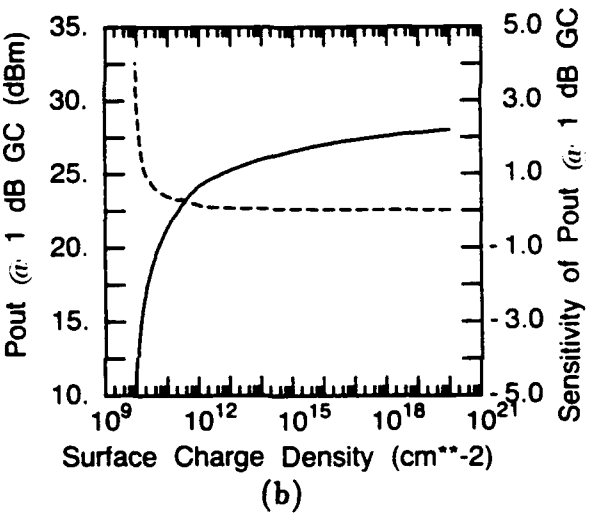


Figure C.15: The effect of parasitic source inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





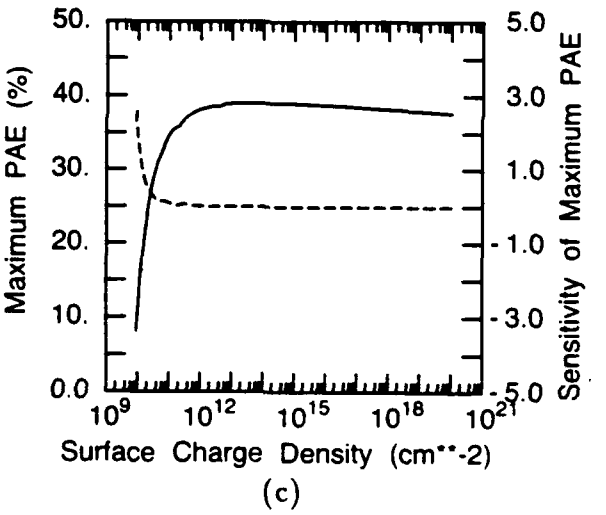
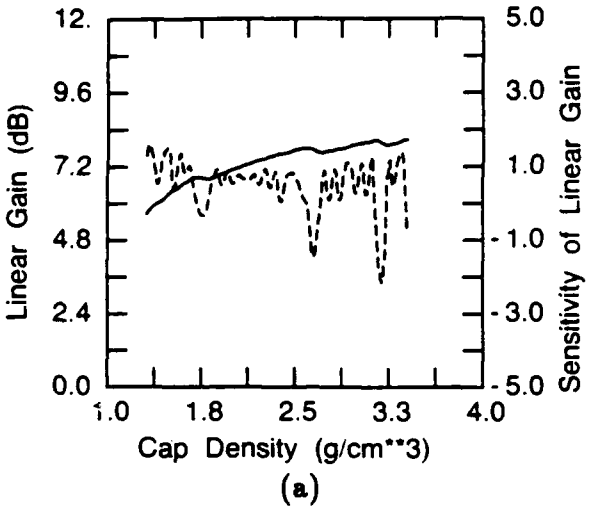
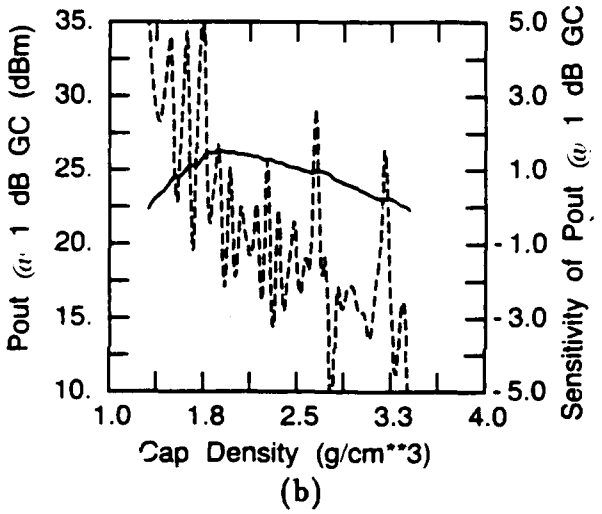


Figure C.16: The effect of surface charge density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





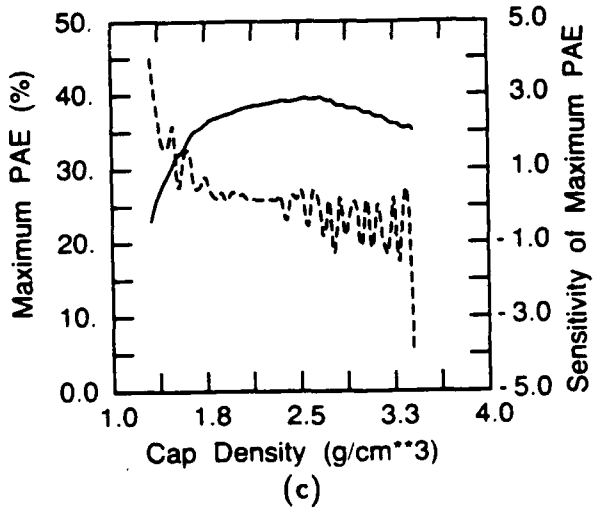
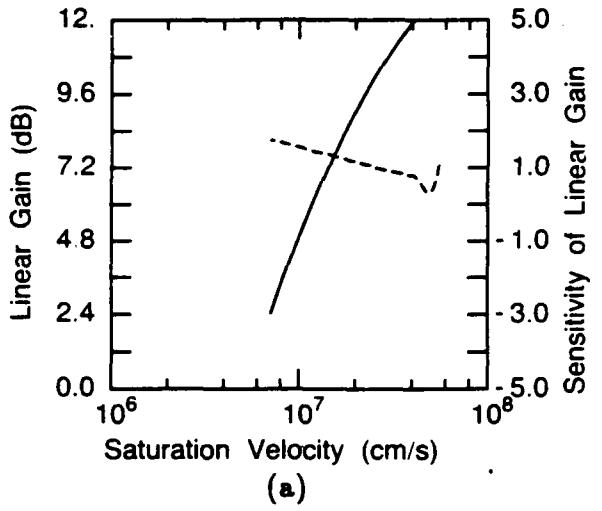
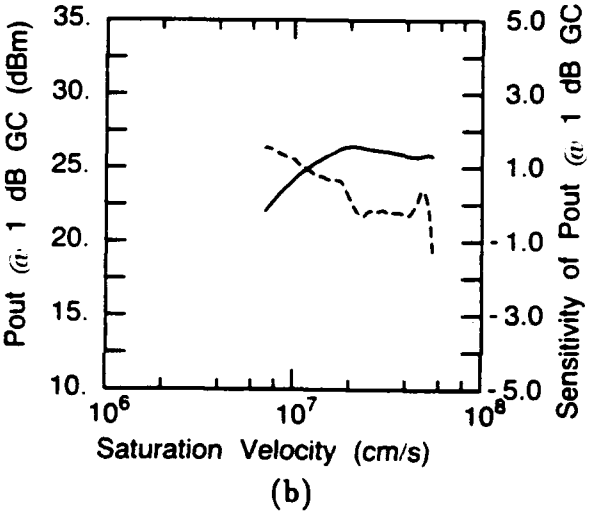


Figure C.17: The effect of density of implant cap variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





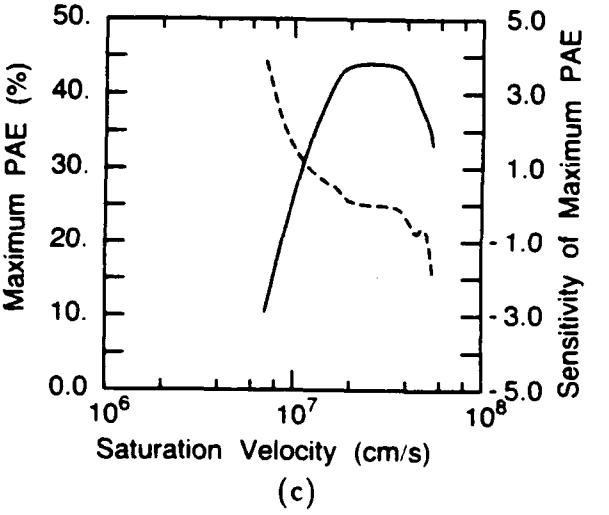
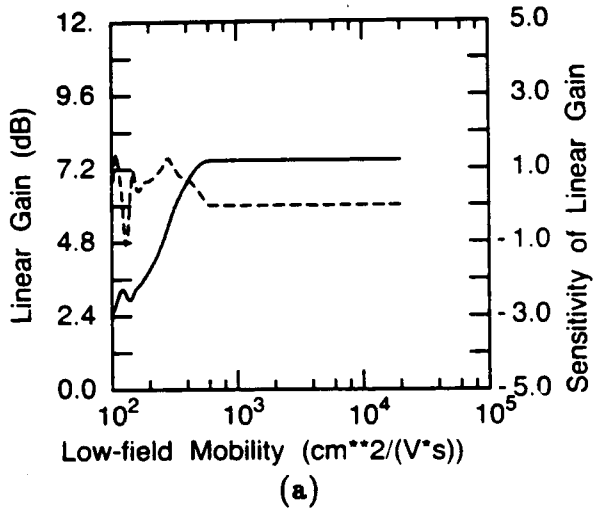
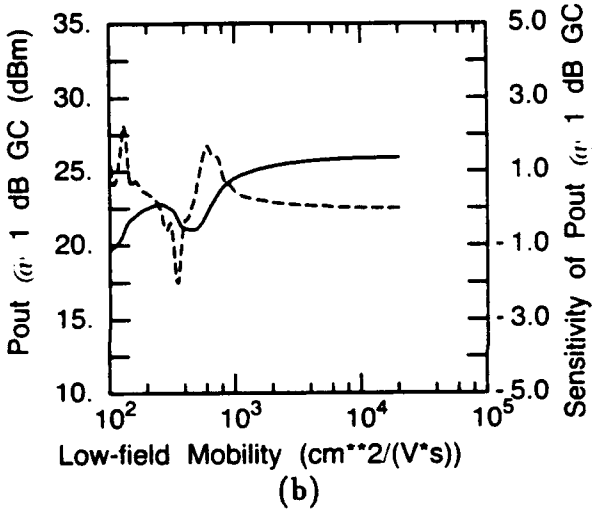


Figure C.18: The effect of electron saturation velocity variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





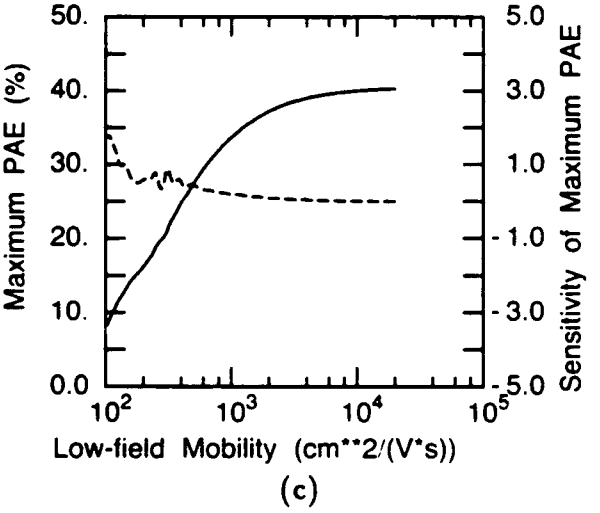
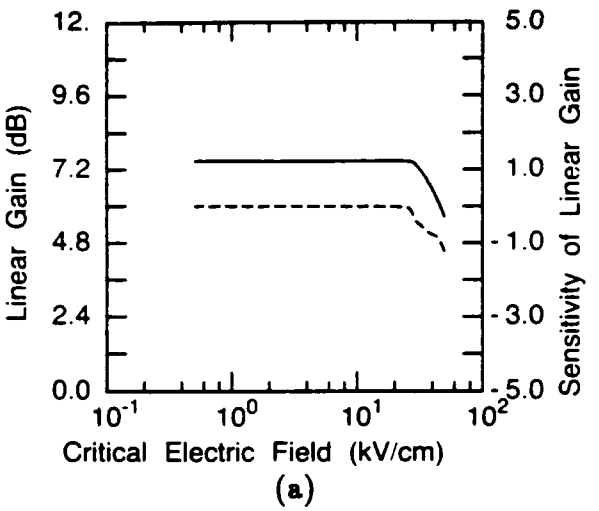
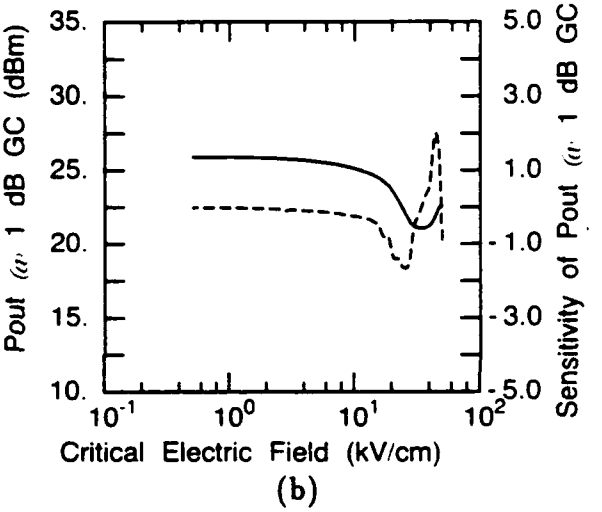


Figure C.19: The effect of electron low-field mobility variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





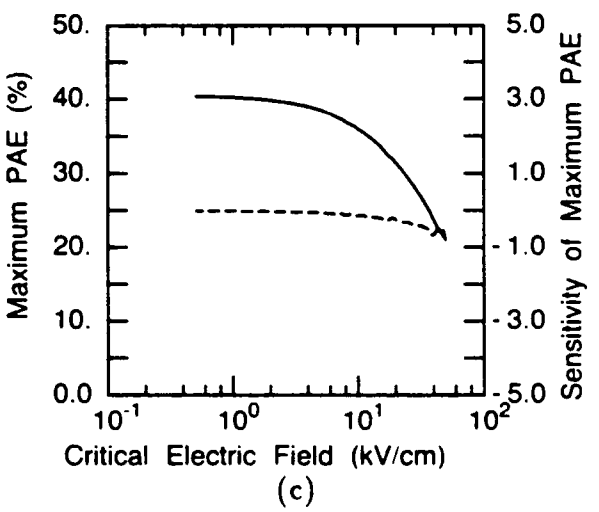
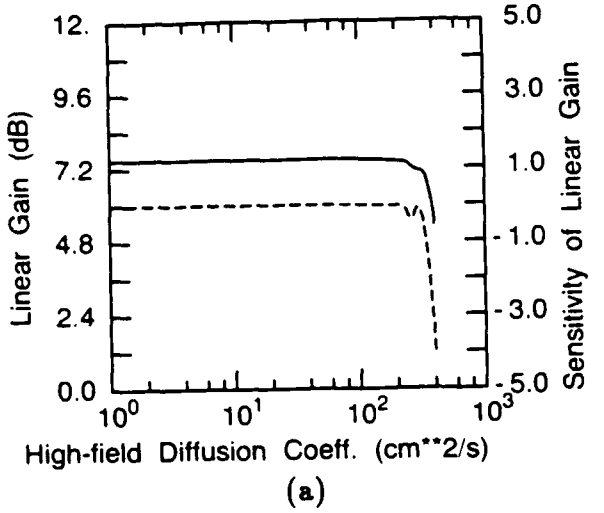
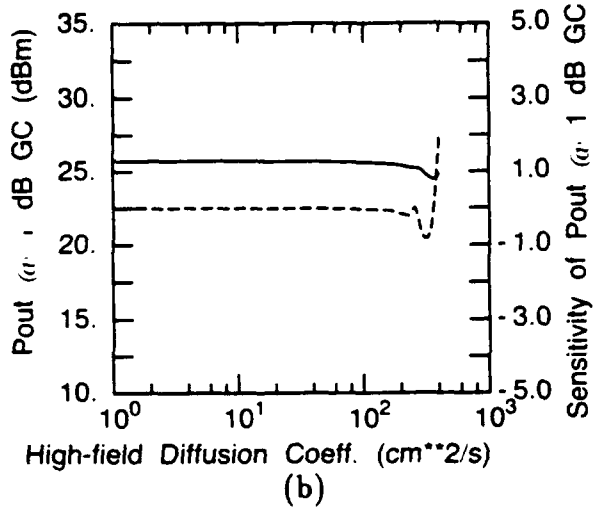


Figure C.20: The effect of electron critical electric field variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





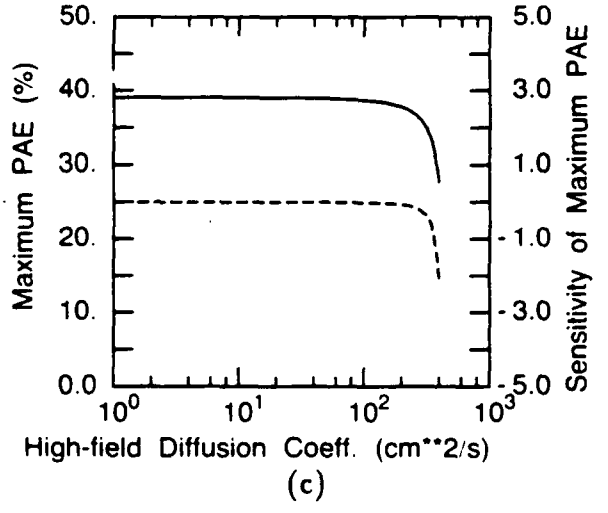
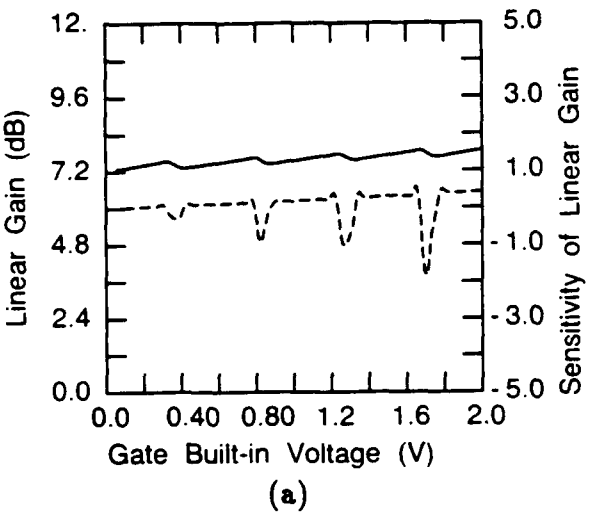
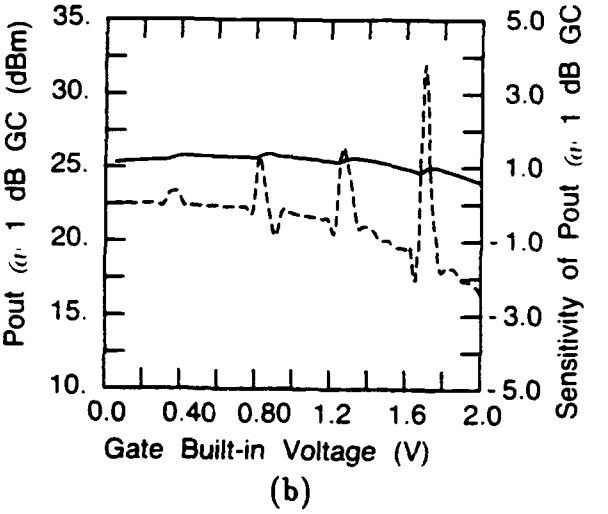


Figure C.21: The effect of electron high-field diffusion coefficient variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





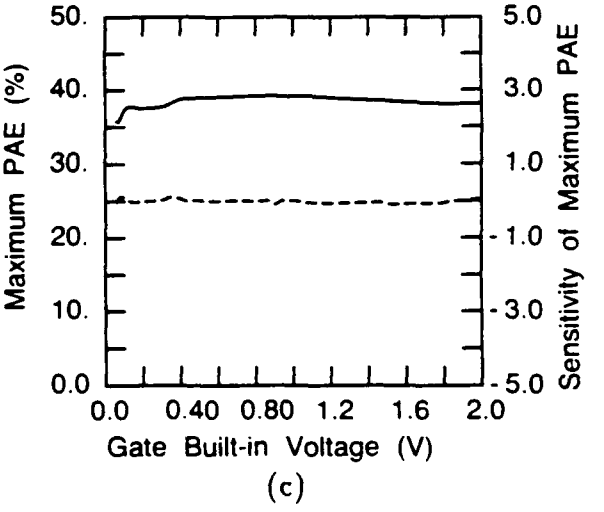


Figure C.22: The effect of gate built-in voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

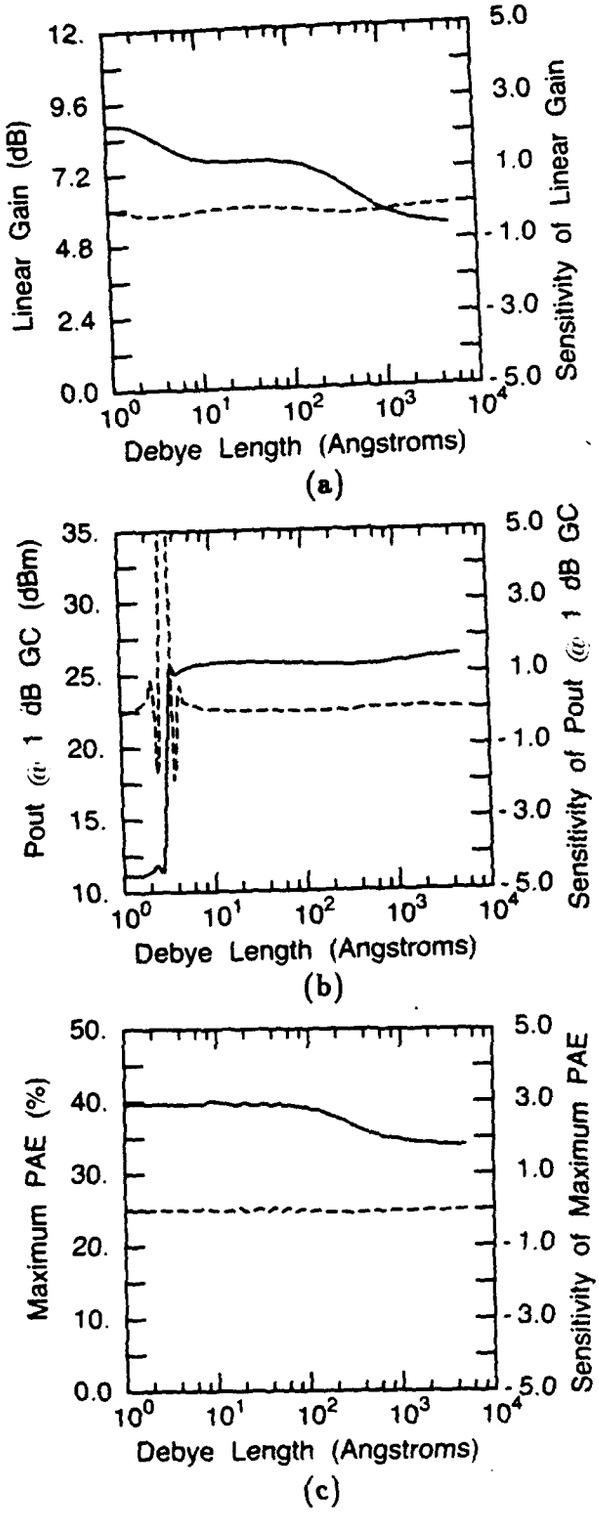
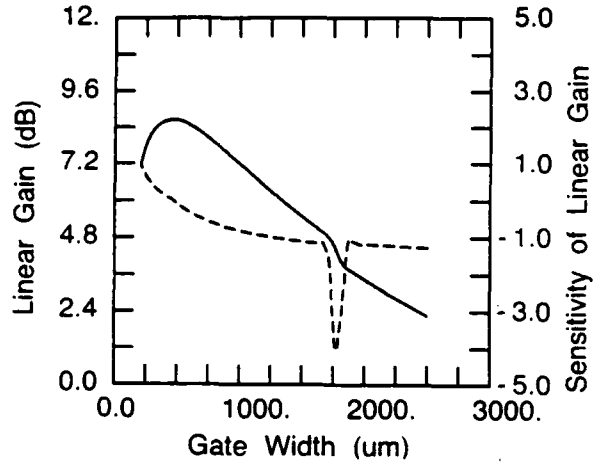


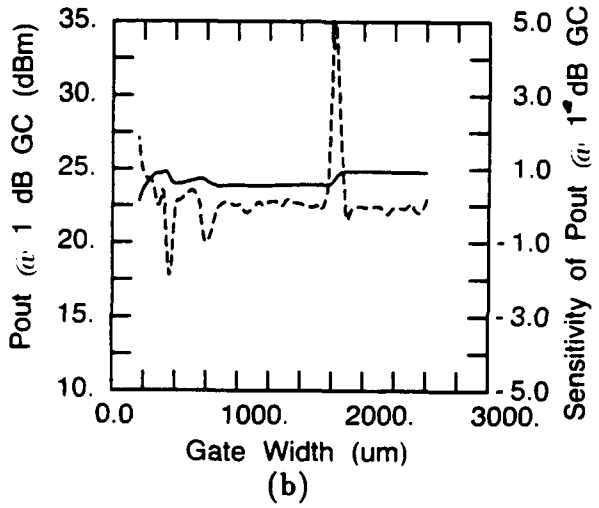
Figure C.23: The effect of Debye length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

Appendix D

Sensitivity Analysis of Buried Channel Device

The data presented in this Appendix is an sensitivity analysis of a buried channel MESFET device. The study was undertaken to identify the parameters to which certain performance measures are most sensitive. The performance measures considered were the small-signal transducer gain, the output power at 1 dB transducer gain compression, and the maximum transducer power-added efficiency. These measures are most sensitive to gate length, gate width, thicknesses and doping densities of the high and low doped regions, gate-source voltage, and drain-source voltage. During the simulations for which the DC bias voltages were not analysis parameters, the gate-source bias voltage was set to $0.5V_{po}$, and the drain-source bias voltage was set to $0.5V_{dsbd}$.





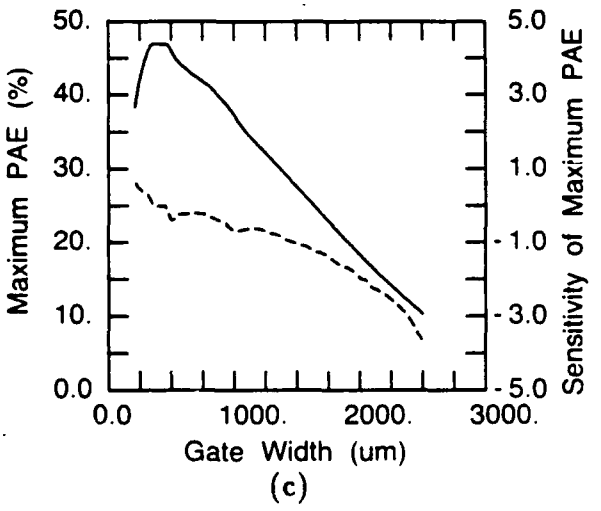
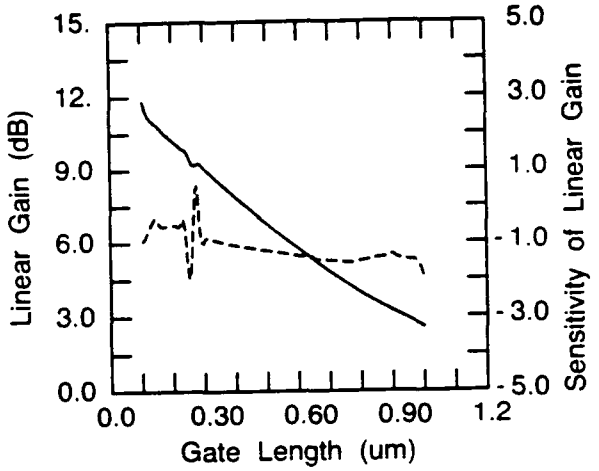
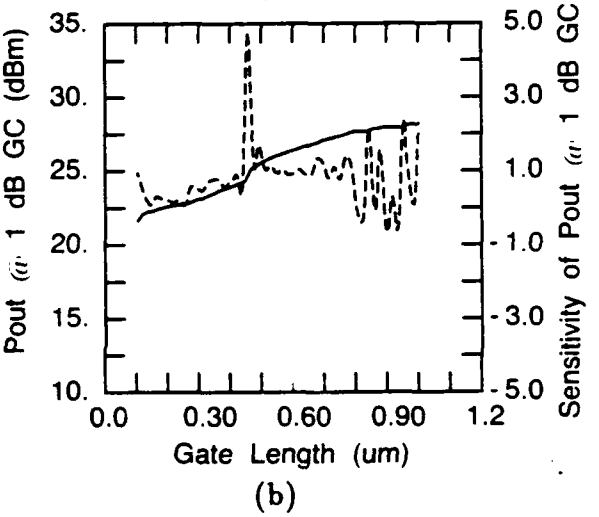


Figure D.1: The effect of gate width variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





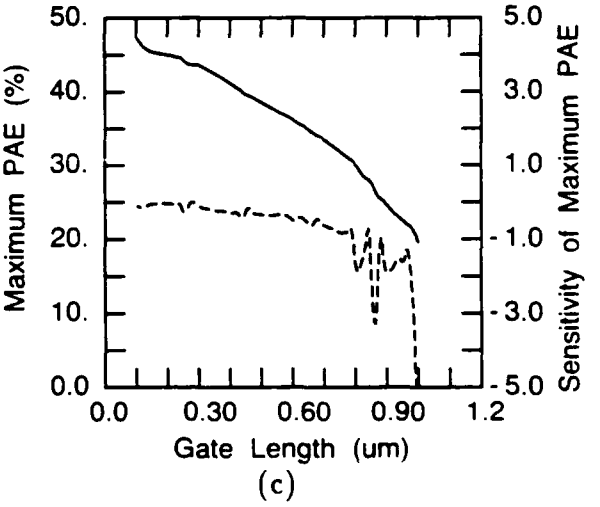
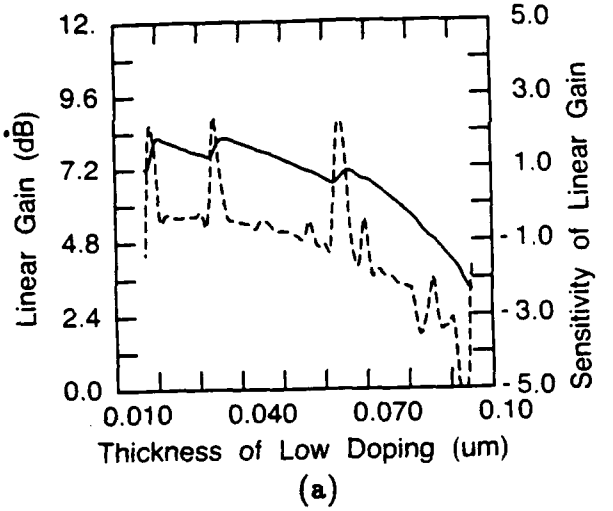
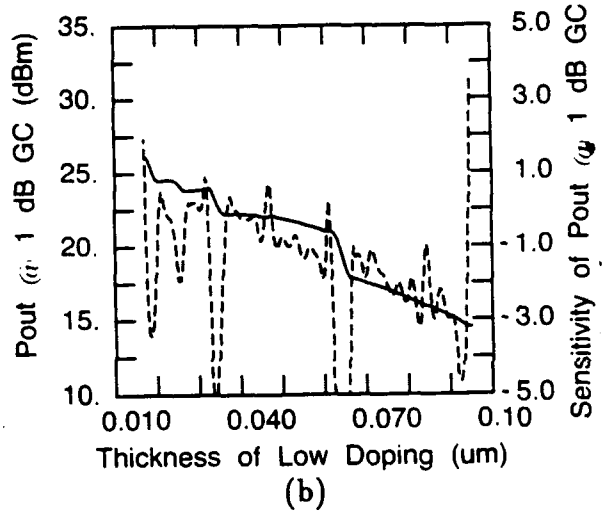


Figure D.2: The effect of gate length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





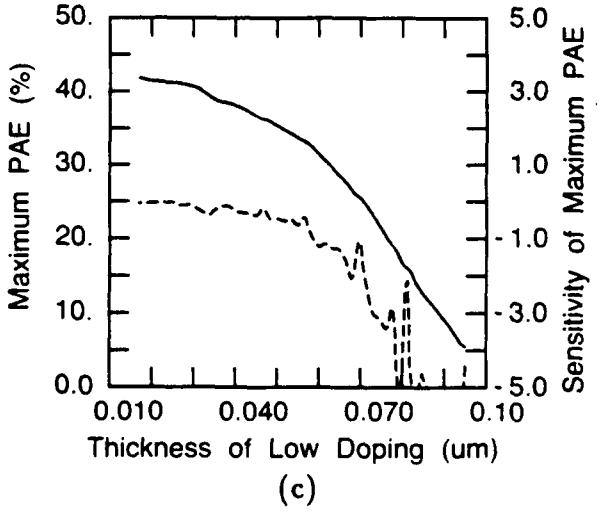
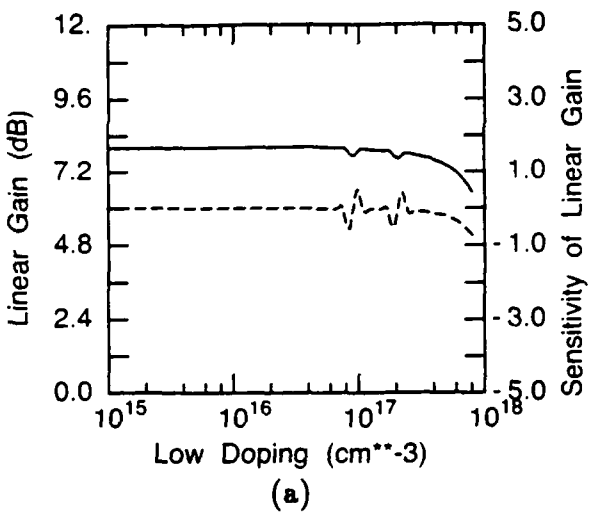
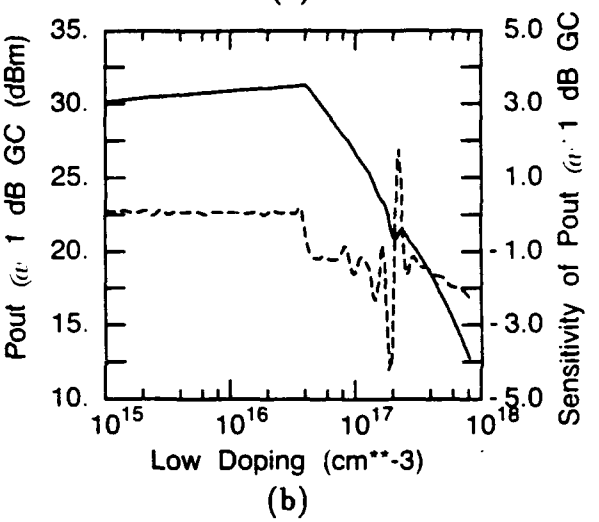


Figure D.3: The effect of low doping region *thickness variation on:* (a) *small-signal* transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





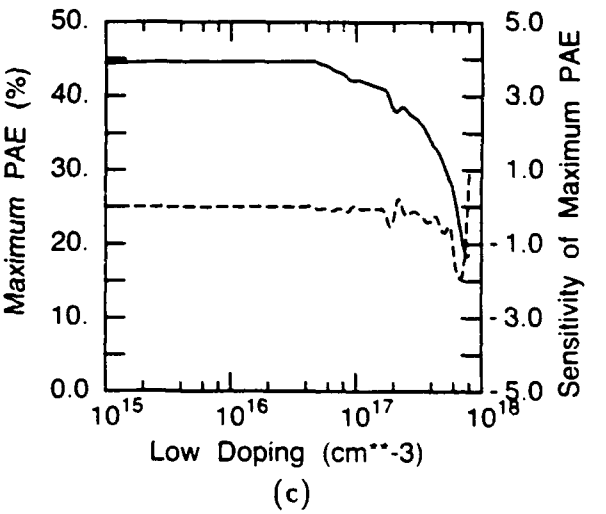
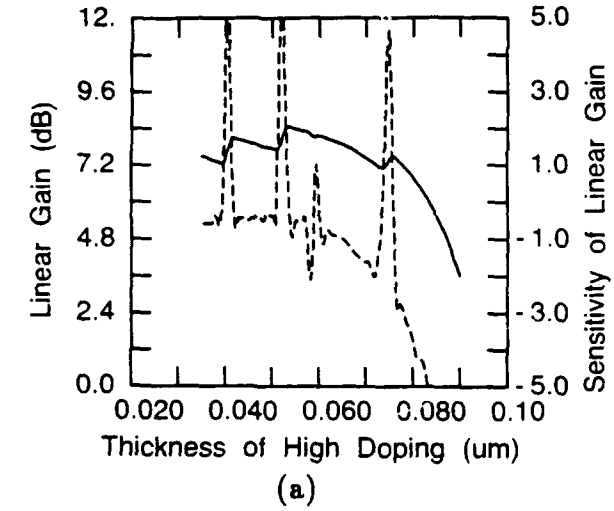
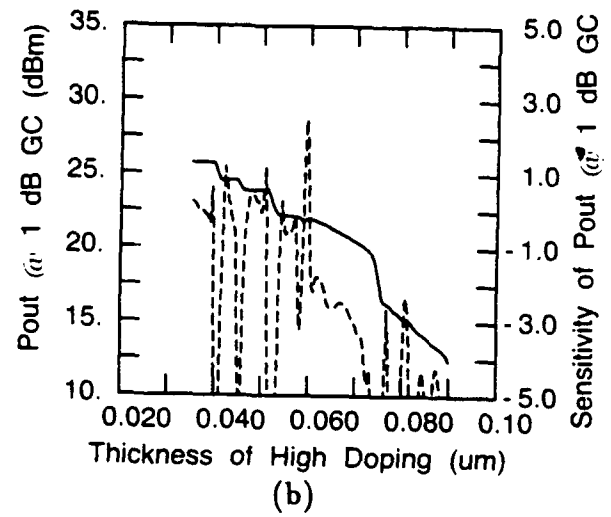


Figure D.4: The effect of low doping density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





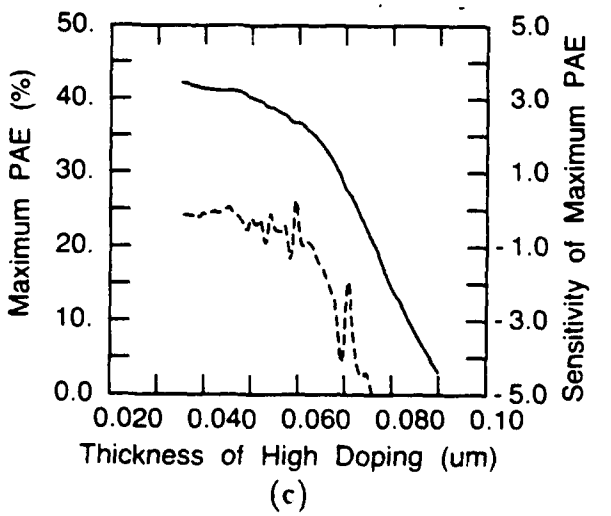
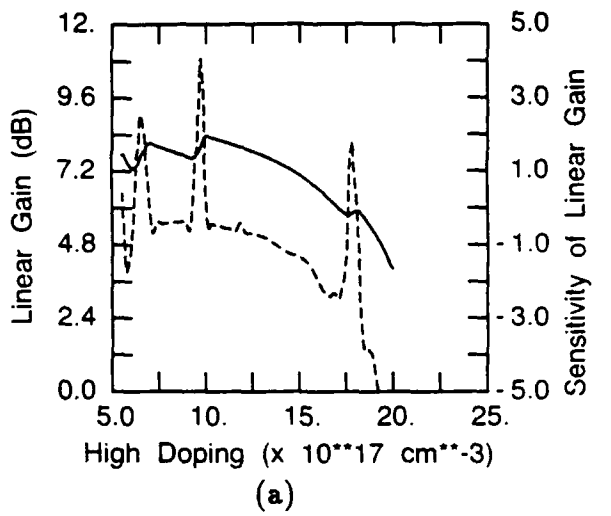
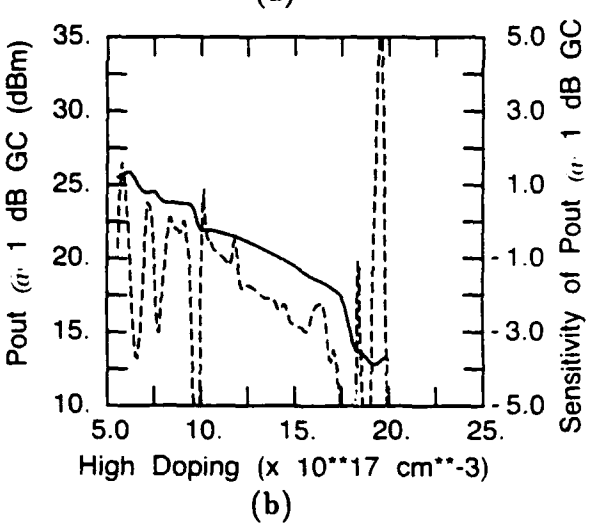


Figure D.5: The effect of high doping region thickness variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





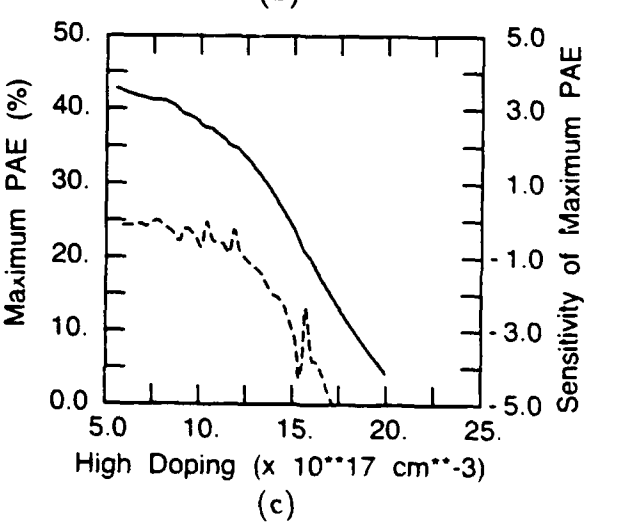
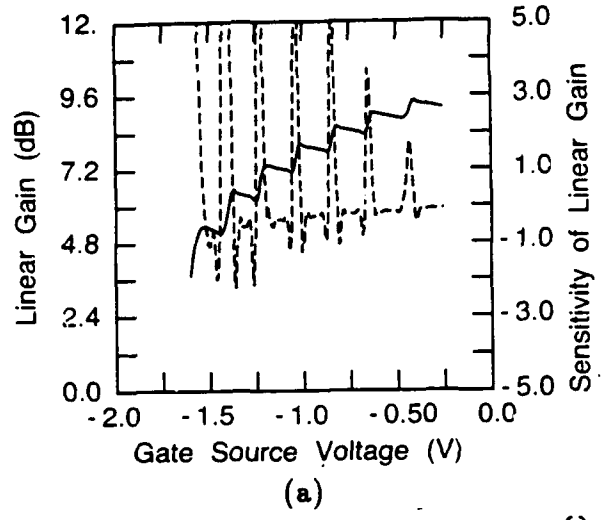
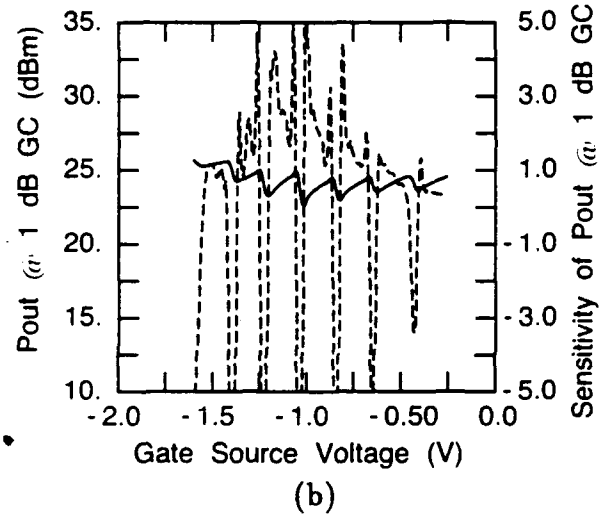


Figure D.6: The effect of high doping density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





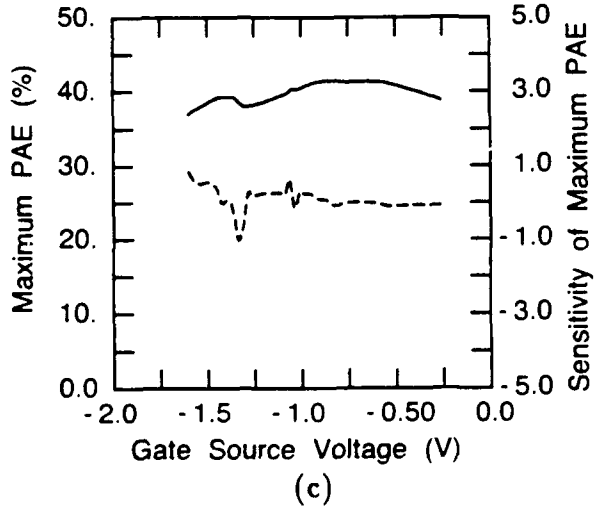
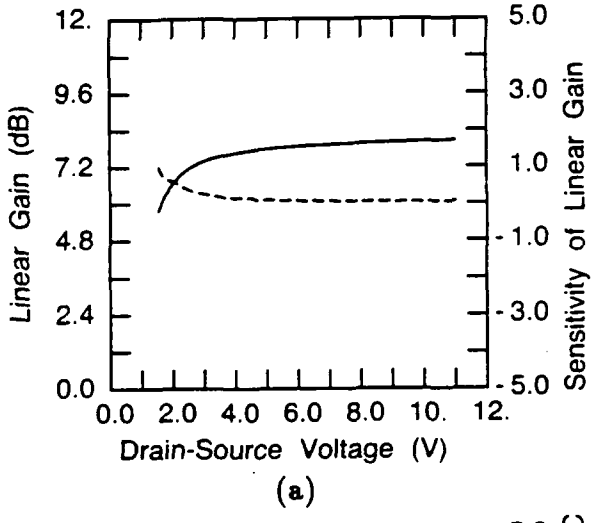
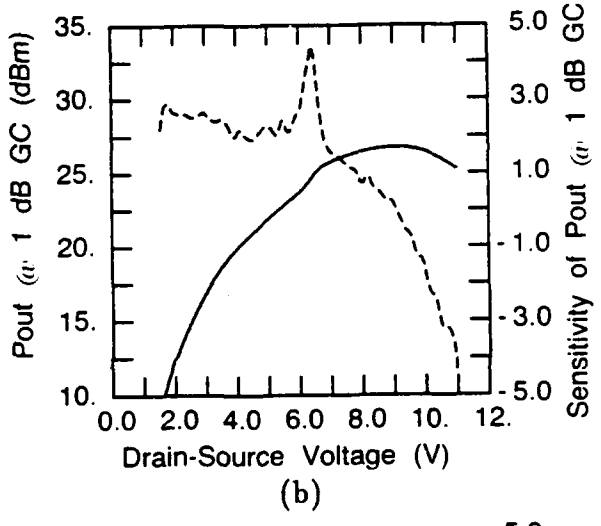


Figure D.7: The effect of DC gate-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





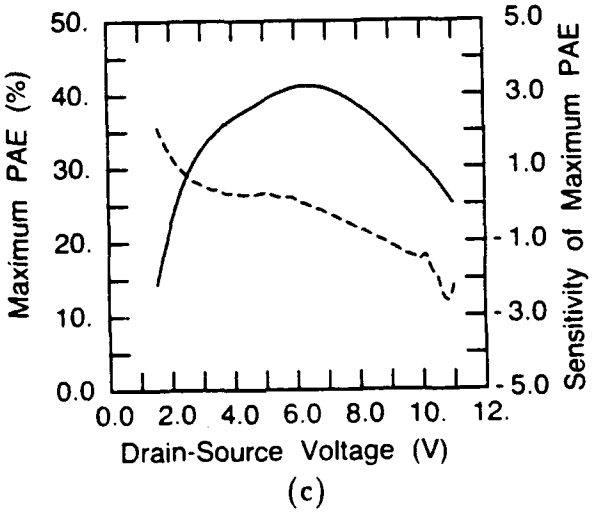
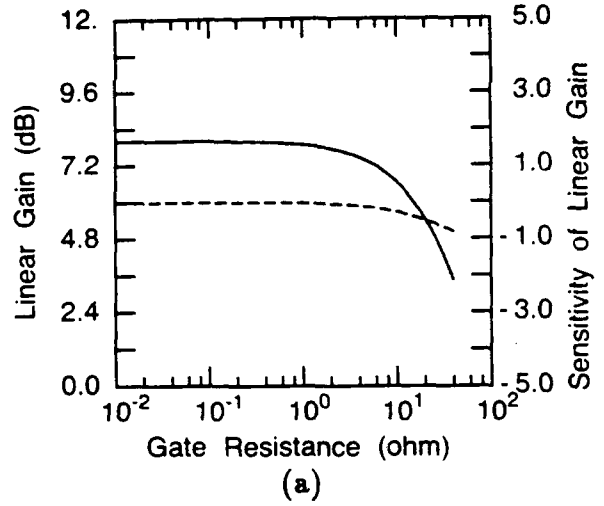
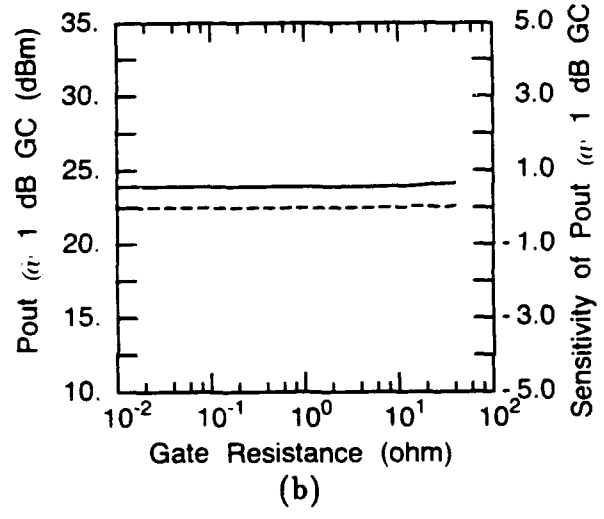


Figure D.8: The effect of DC drain-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





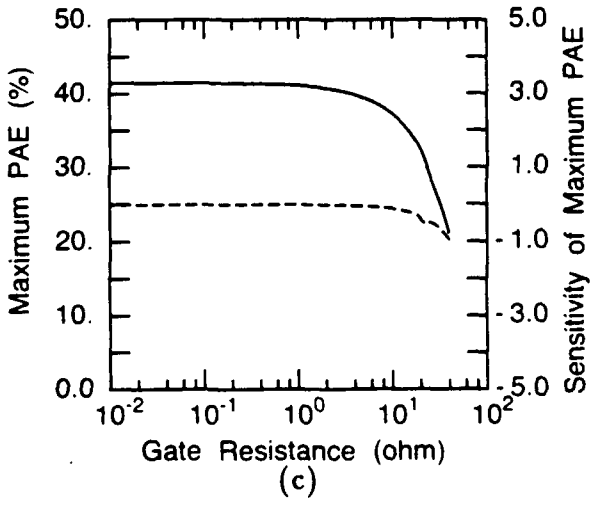
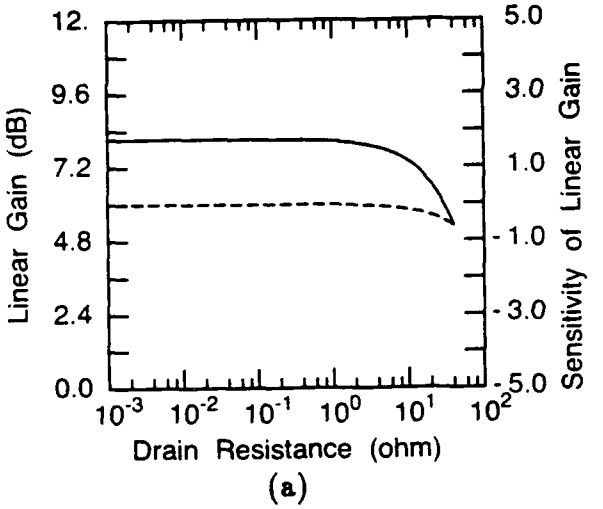
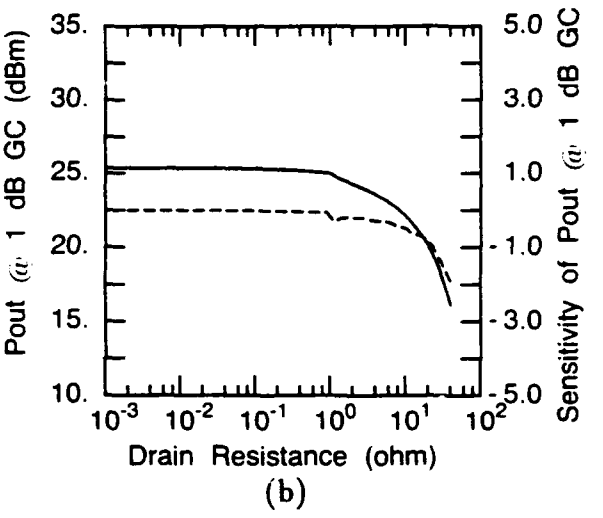


Figure D.9: The effect of parasitic gate resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





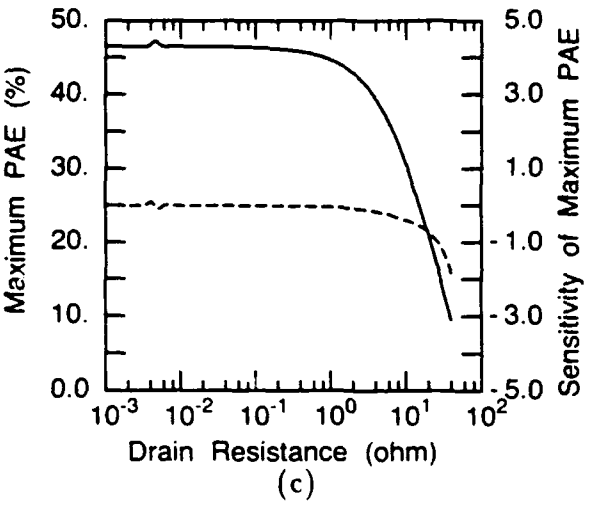
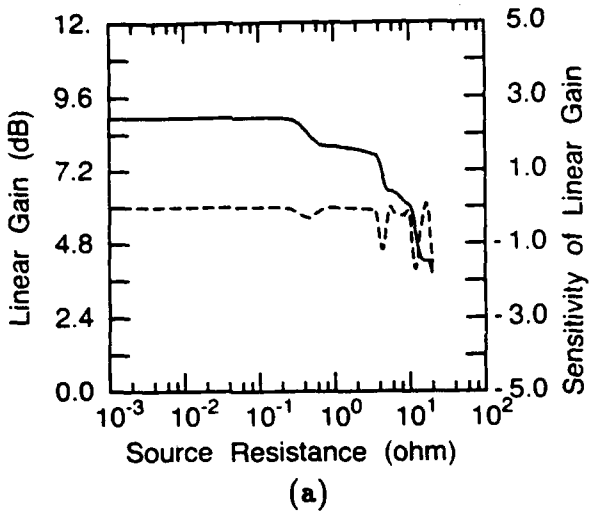
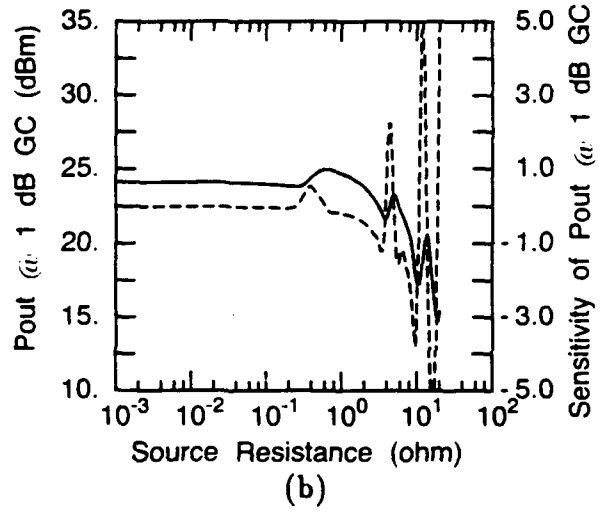


Figure D.10: The effect of parasitic drain resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





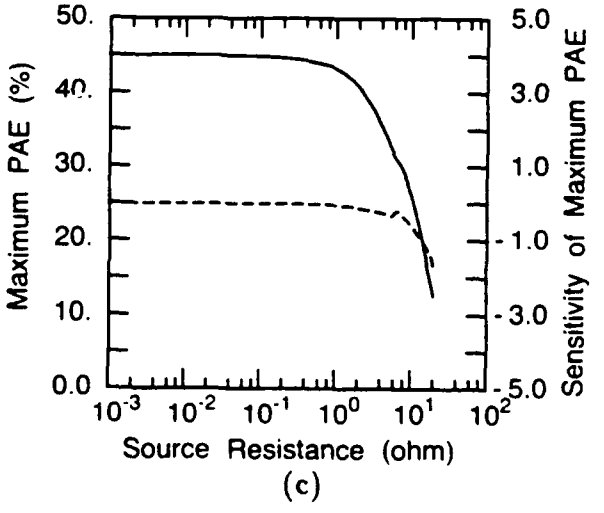
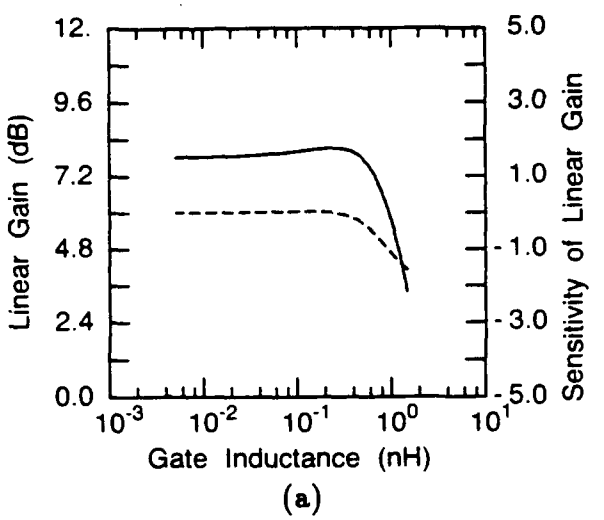
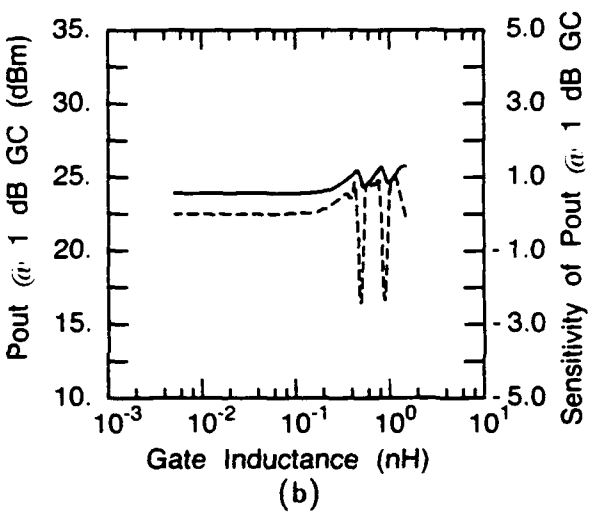


Figure D.11: The effect of parasitic source resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





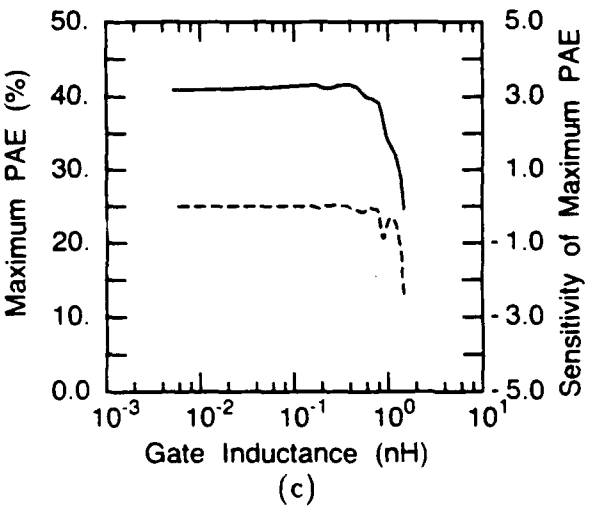
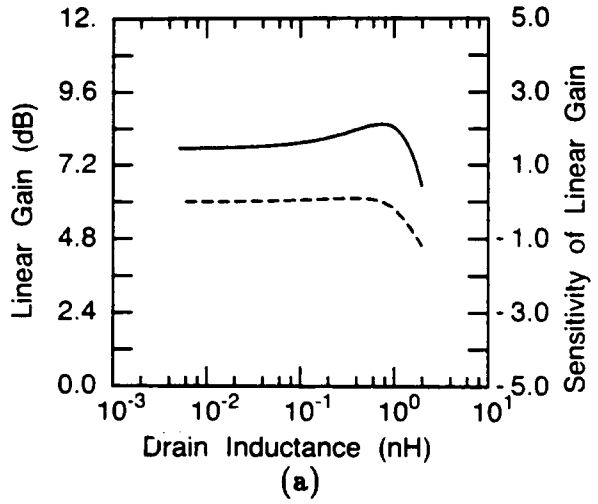
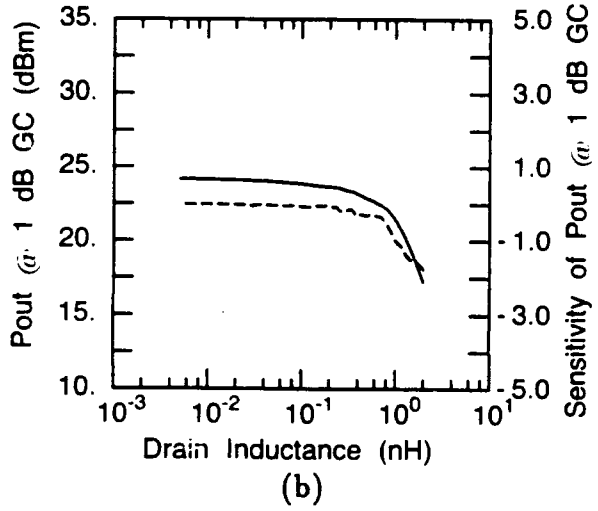


Figure D.12: The effect of parasitic gate inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





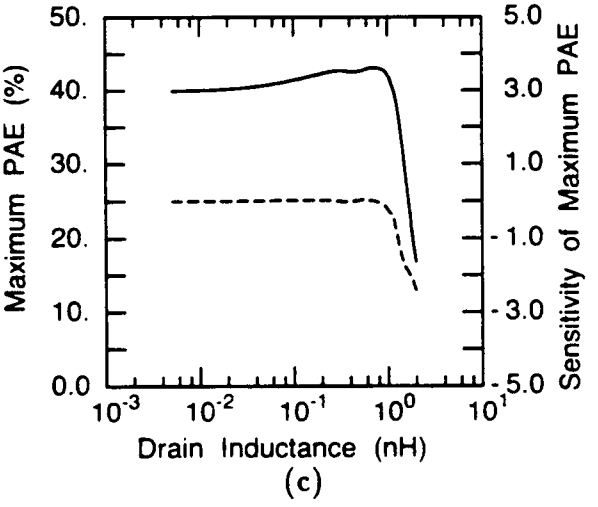
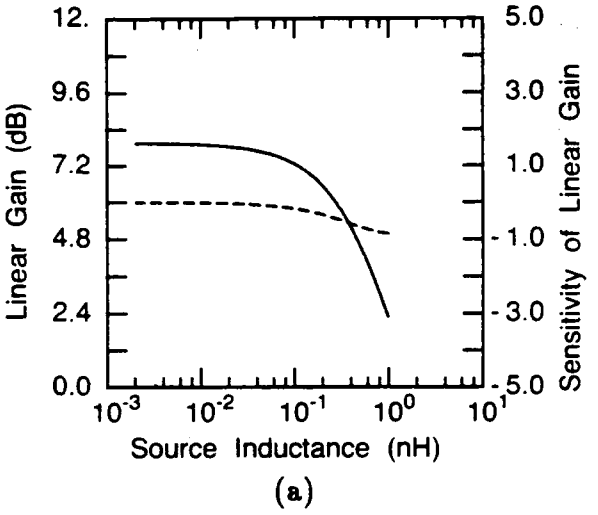
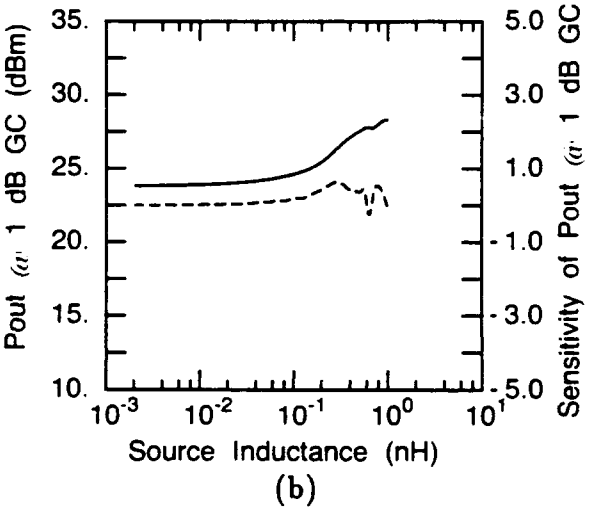


Figure D.13: The effect of parasitic drain inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





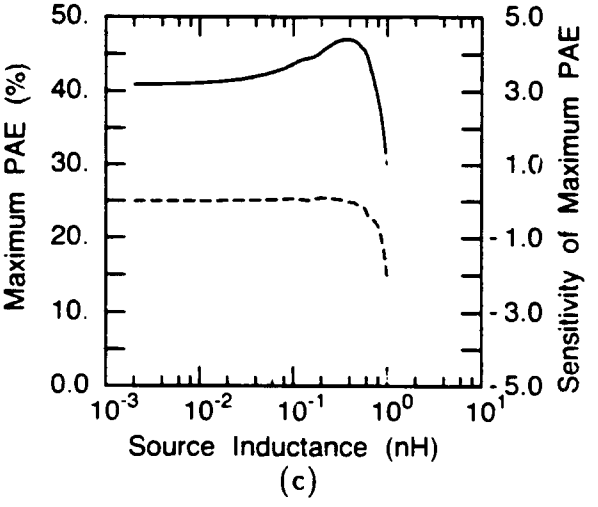
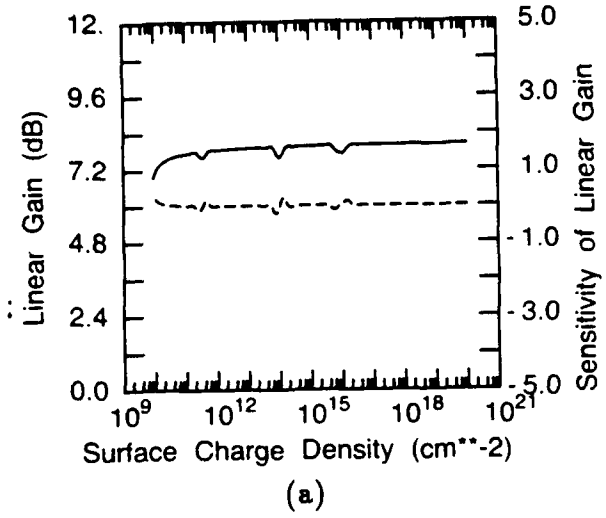
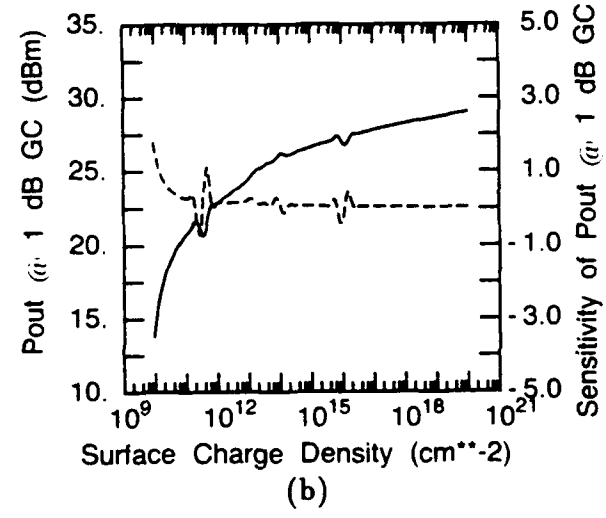


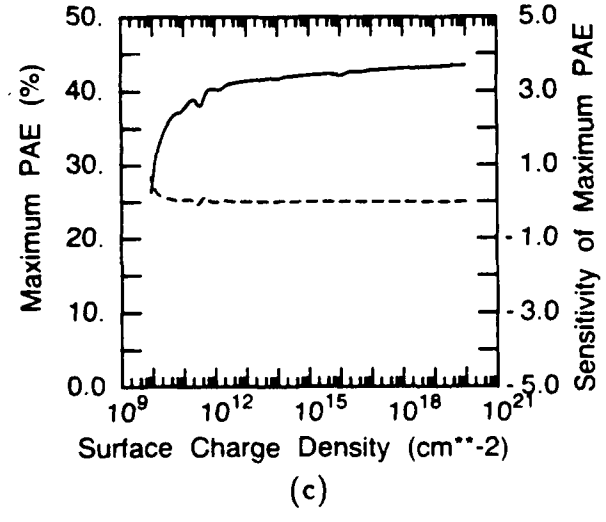
Figure D.14: The effect of parasitic source inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.



(a)

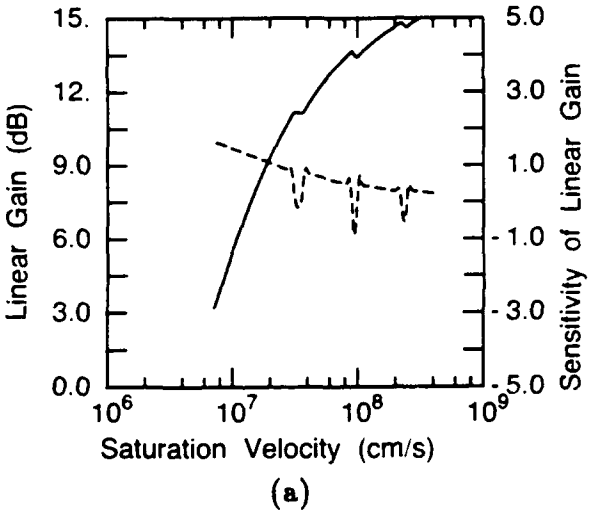


(b)

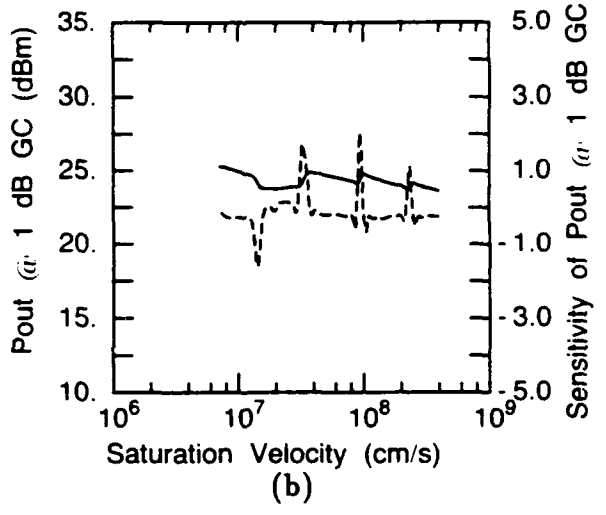


(c)

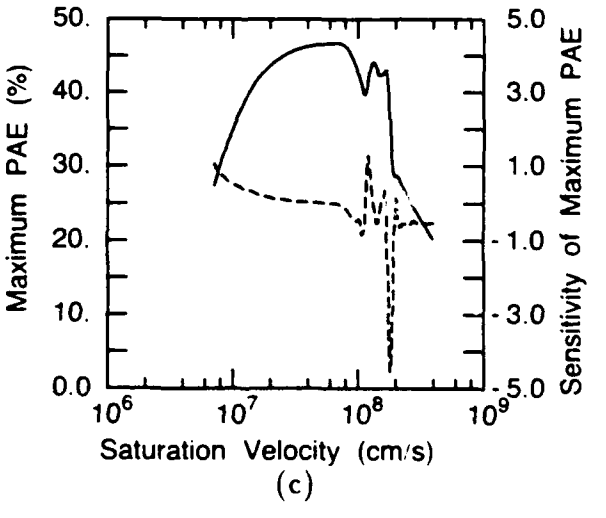
Figure D.15: The effect of surface charge density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.



(a)

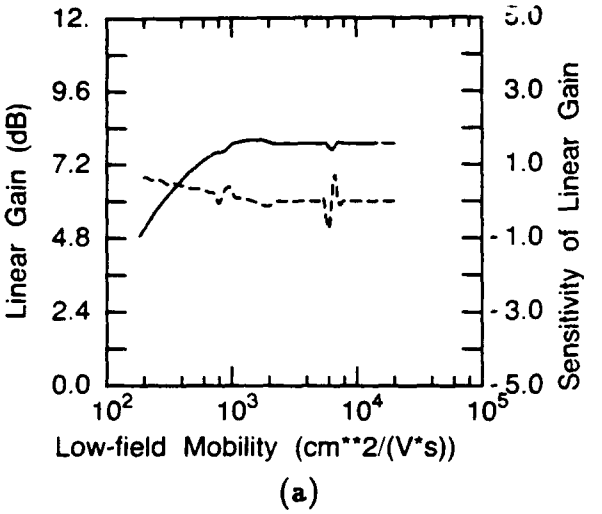


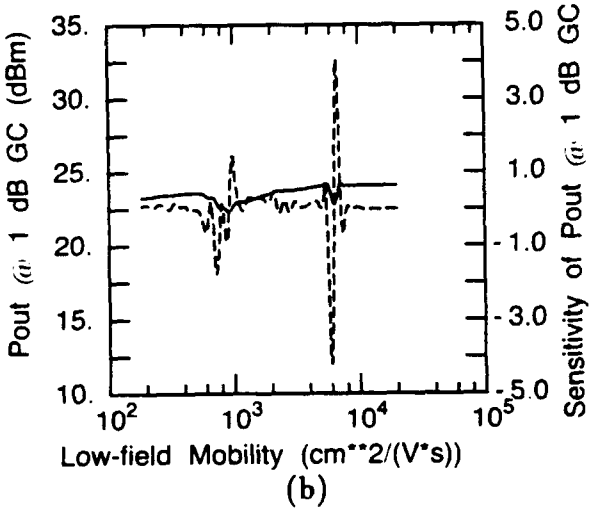
(b)



(c)

Figure D.16: The effect of electron saturation velocity variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





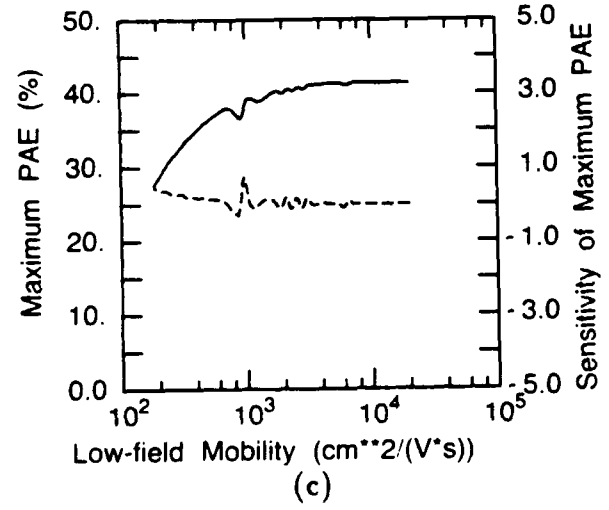
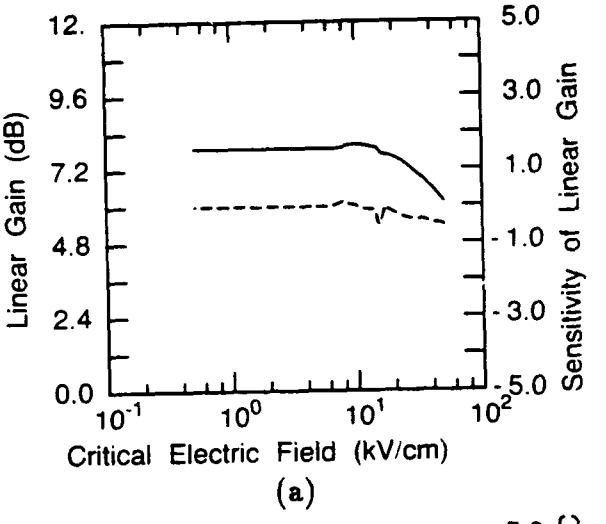
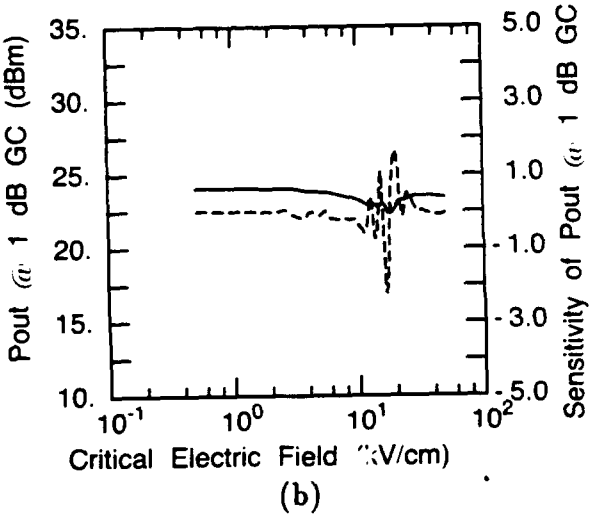


Figure D.17: The effect of electron low-field mobility variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





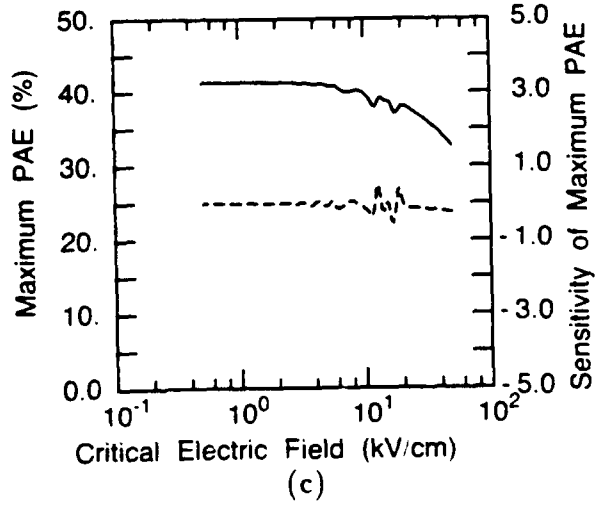
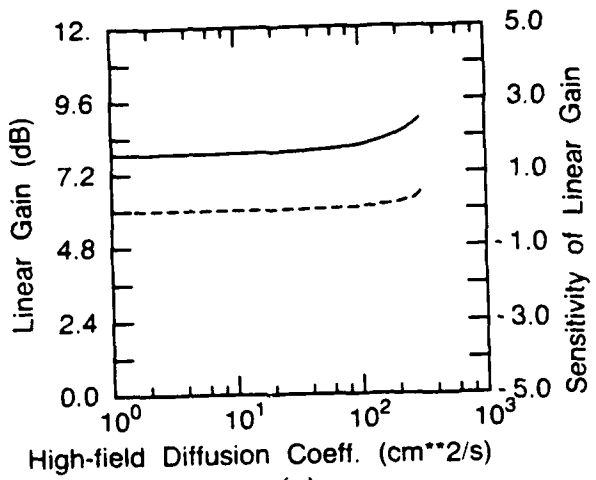
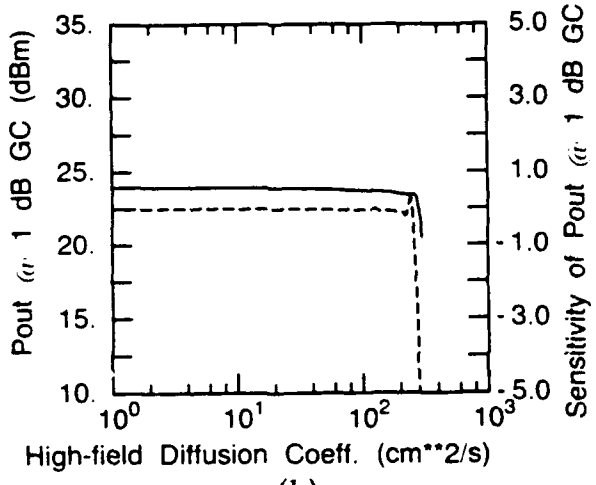


Figure D.18: The effect of electron critical electric field variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





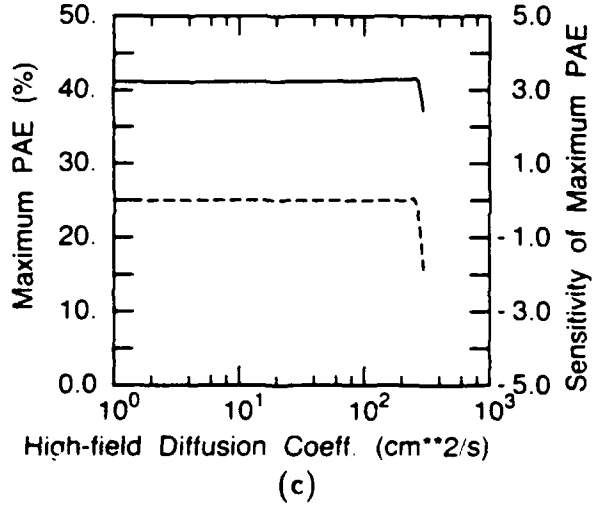
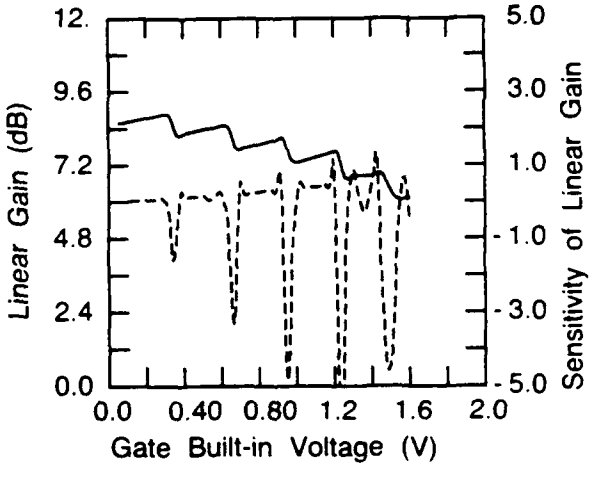
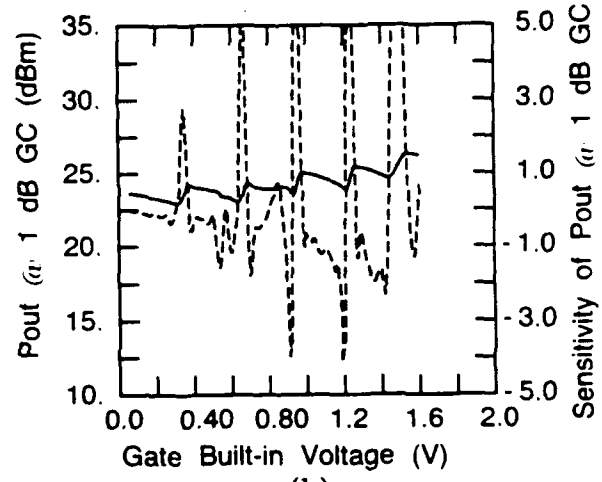


Figure D.19: The effect of electron high-field diffusion coefficient variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





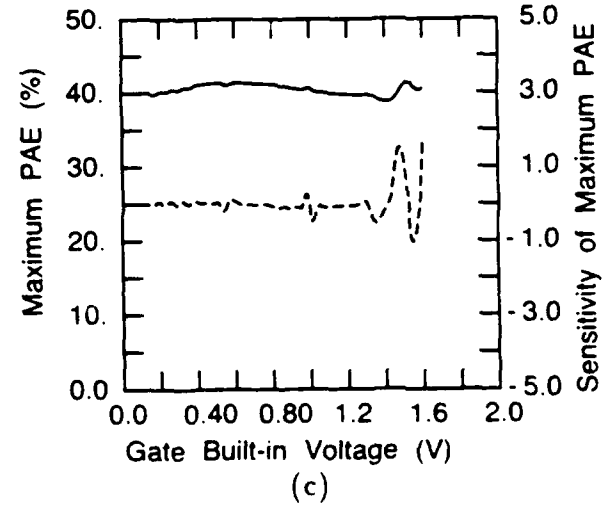


Figure D.20: The effect of gate built-in voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

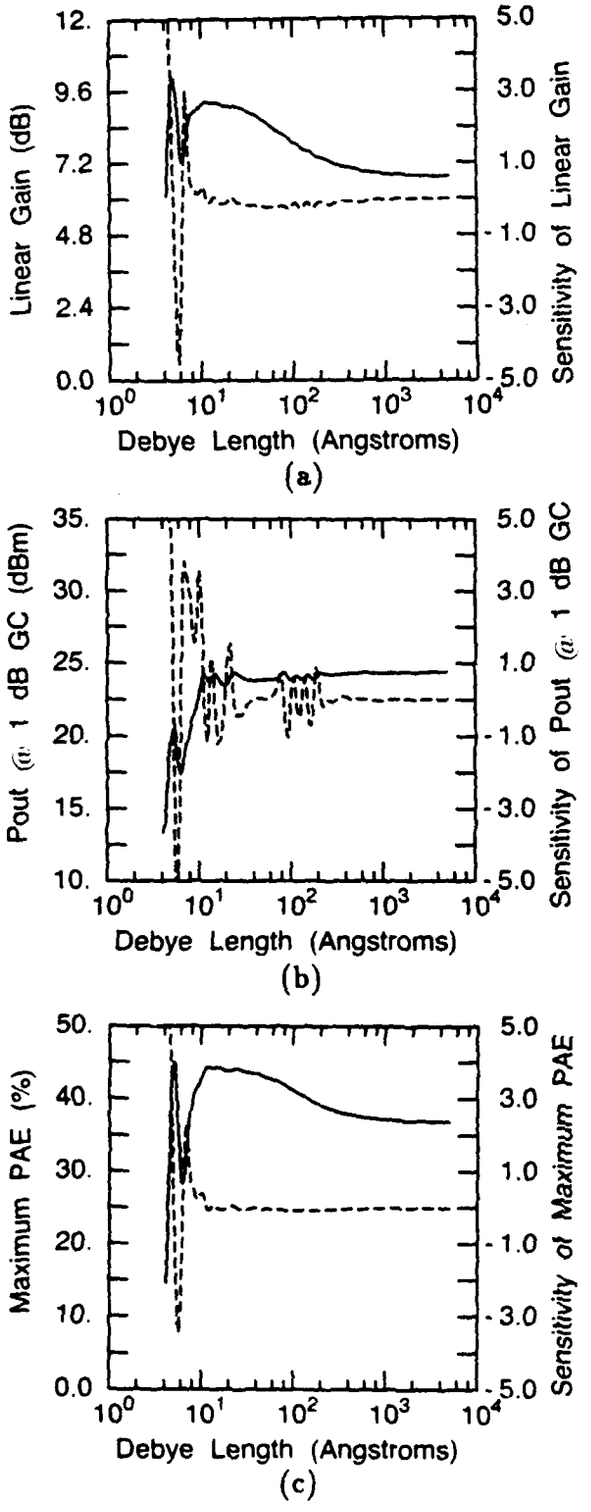


Figure D.21: The effect of Debye length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

Appendix E

Sensitivity Analysis of Uniform Channel Device

The data presented in this Appendix is an sensitivity analysis of a uniform channel MESFET device. The study was undertaken to identify the parameters to which certain performance measures are most sensitive. The performance measures considered were the small-signal transducer gain, the output power at 1 dB transducer gain compression, and the maximum transducer power-added efficiency. These measures are most sensitive to gate length, gate width, channel doping density, channel thickness, gate-source voltage, and drain-source voltage. During the simulations for which the DC bias voltages were not analysis parameters, the gate-source bias voltage was set to $0.5V_{po}$, and the drain-source bias voltage was set to $0.5V_{dsbd}$.

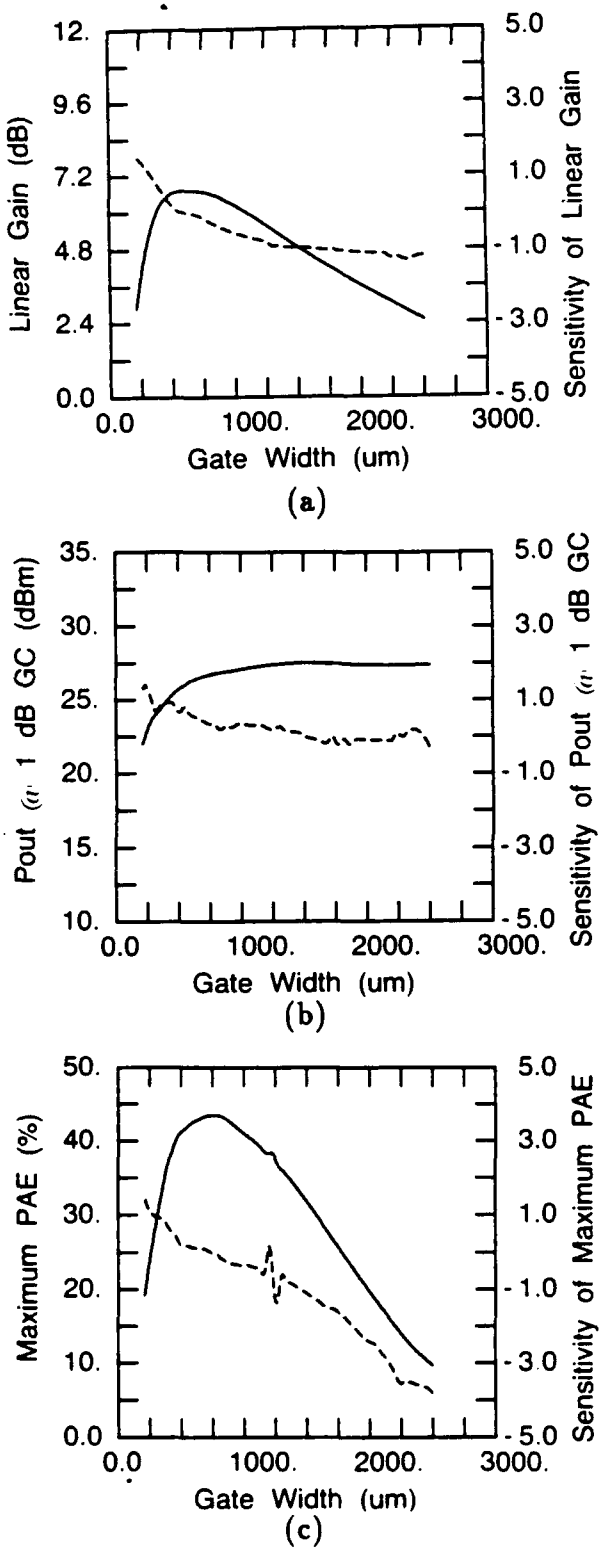


Figure E.1: The effect of gate width variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

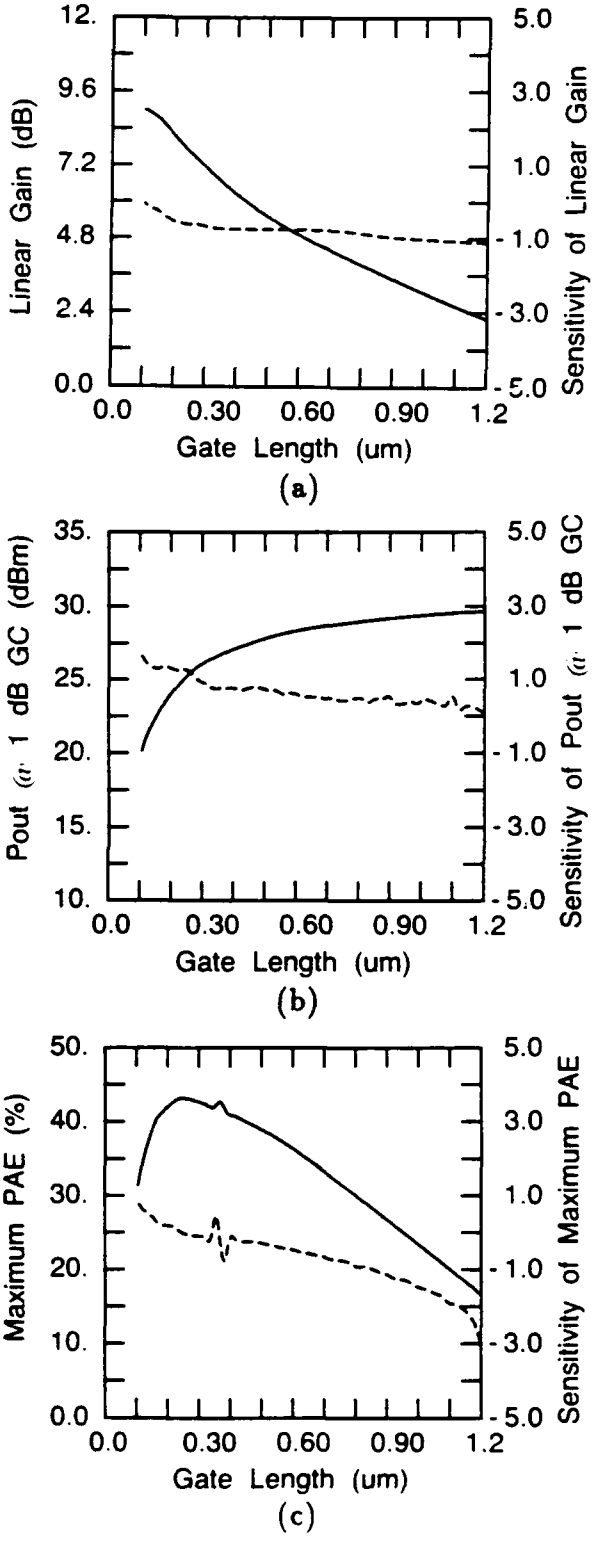
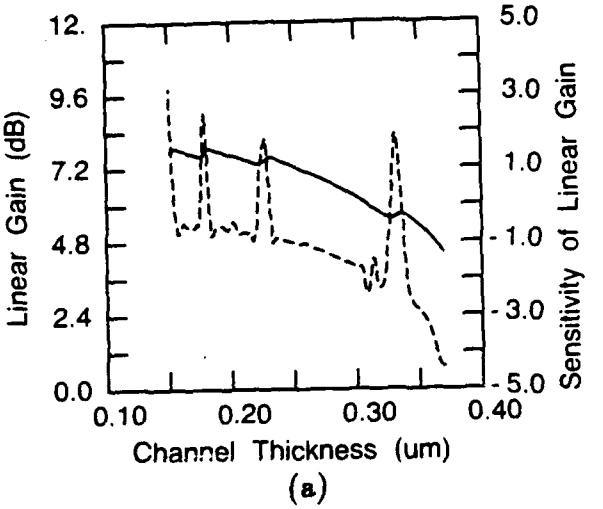
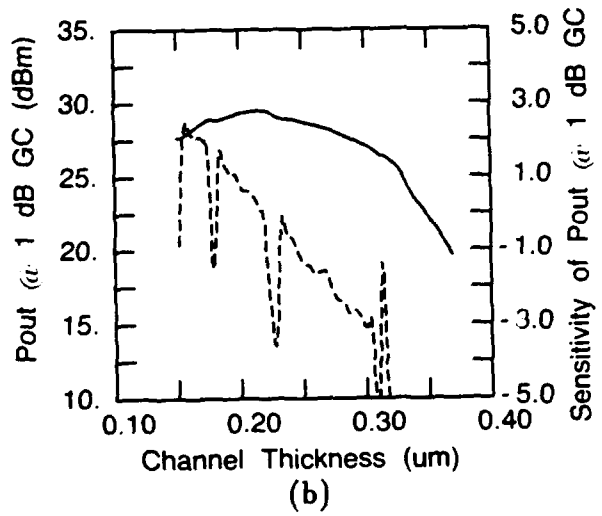


Figure E.2: The effect of gate length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





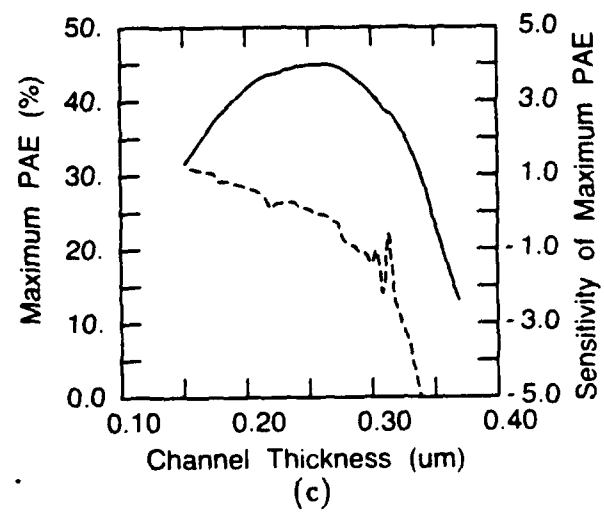
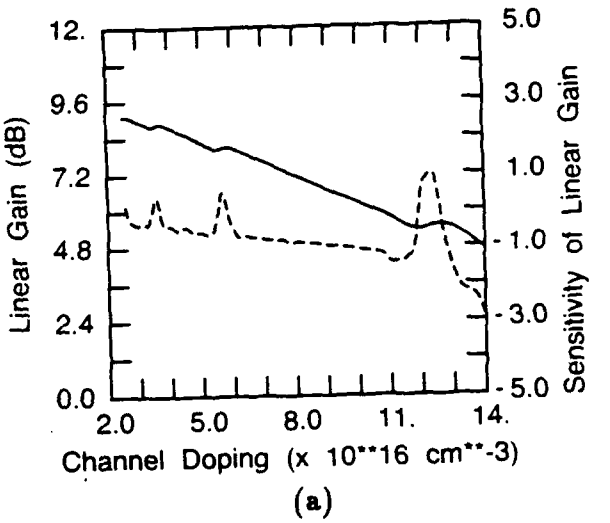
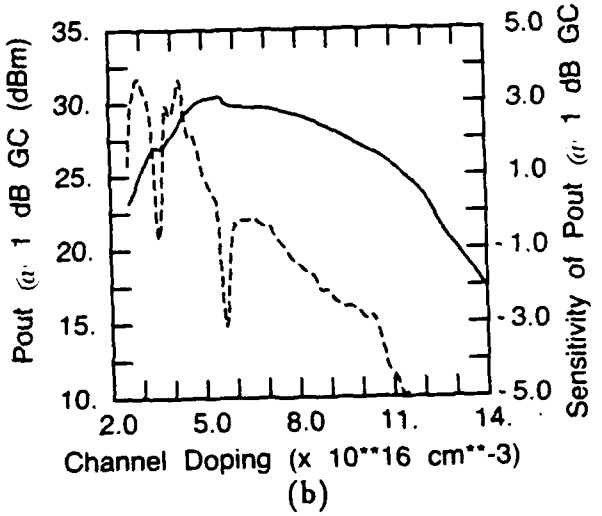


Figure E.3: The effect of channel thickness variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





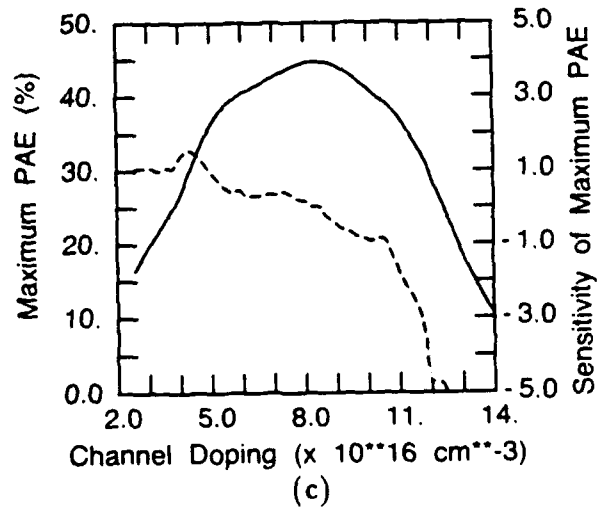


Figure E.4: The effect of channel doping density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

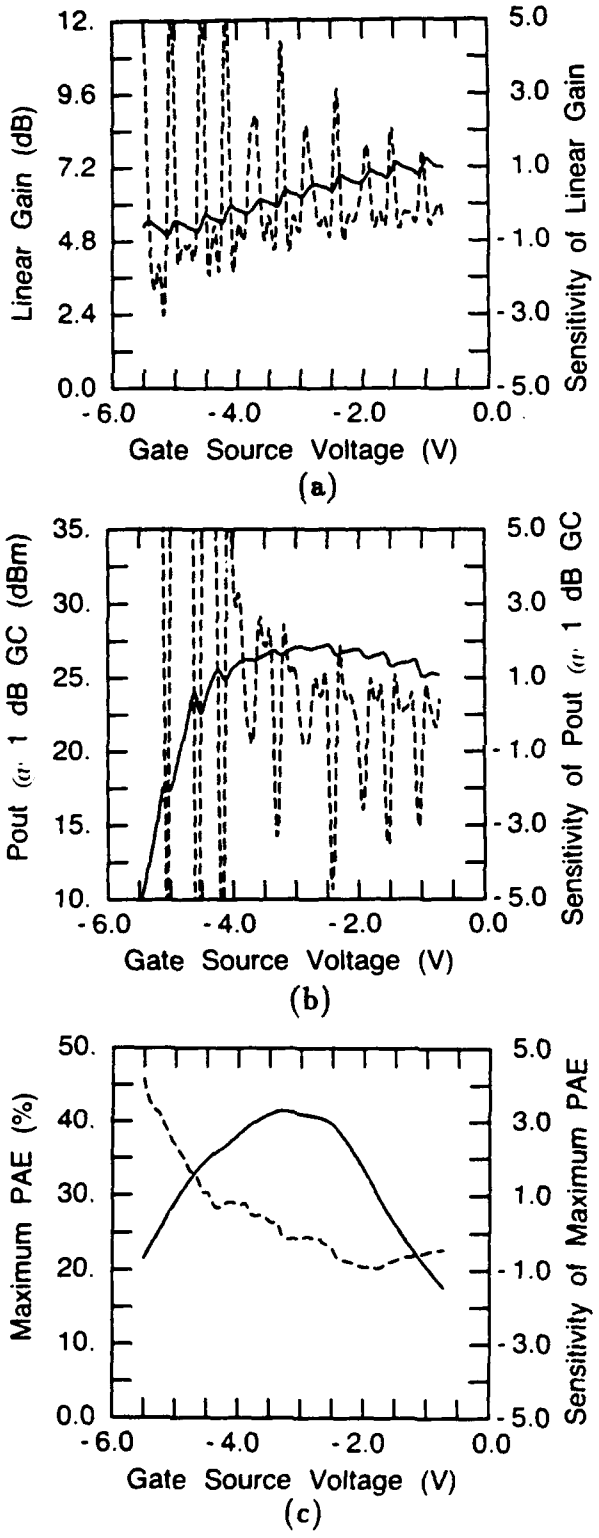


Figure E.5: The effect of DC gate-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

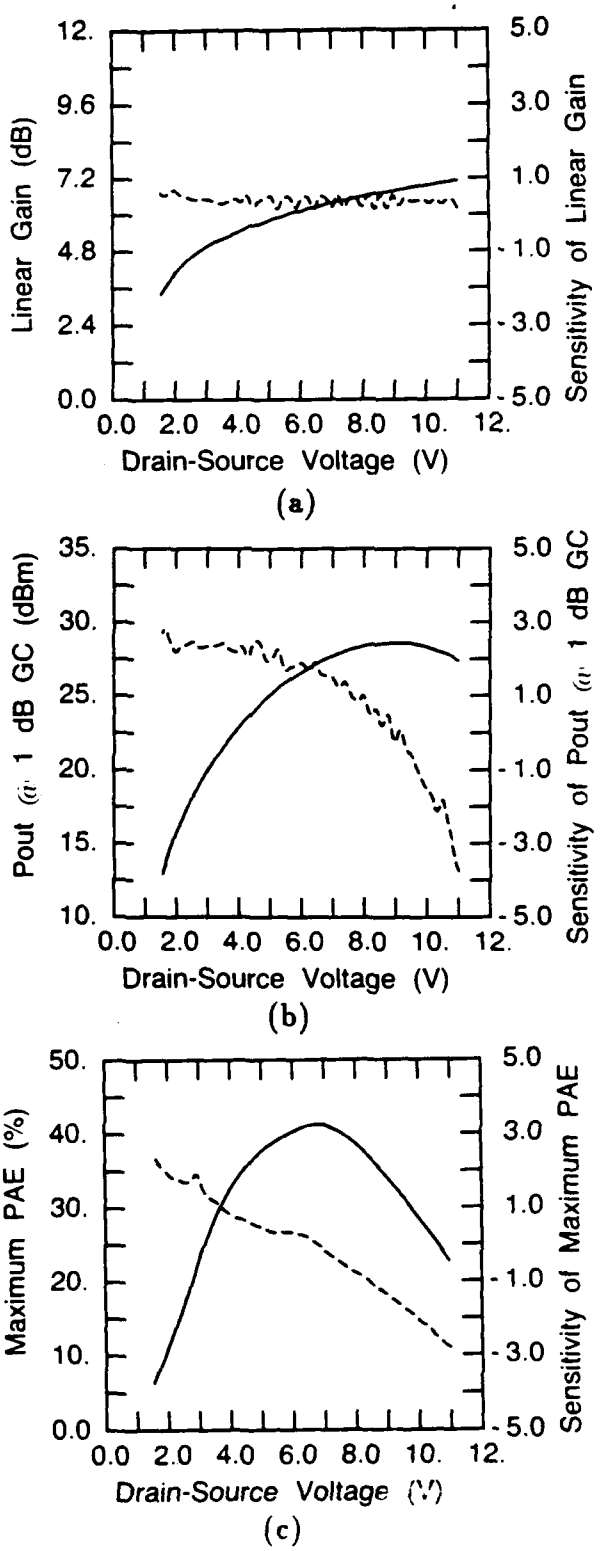


Figure E.6: The effect of DC drain-source bias voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

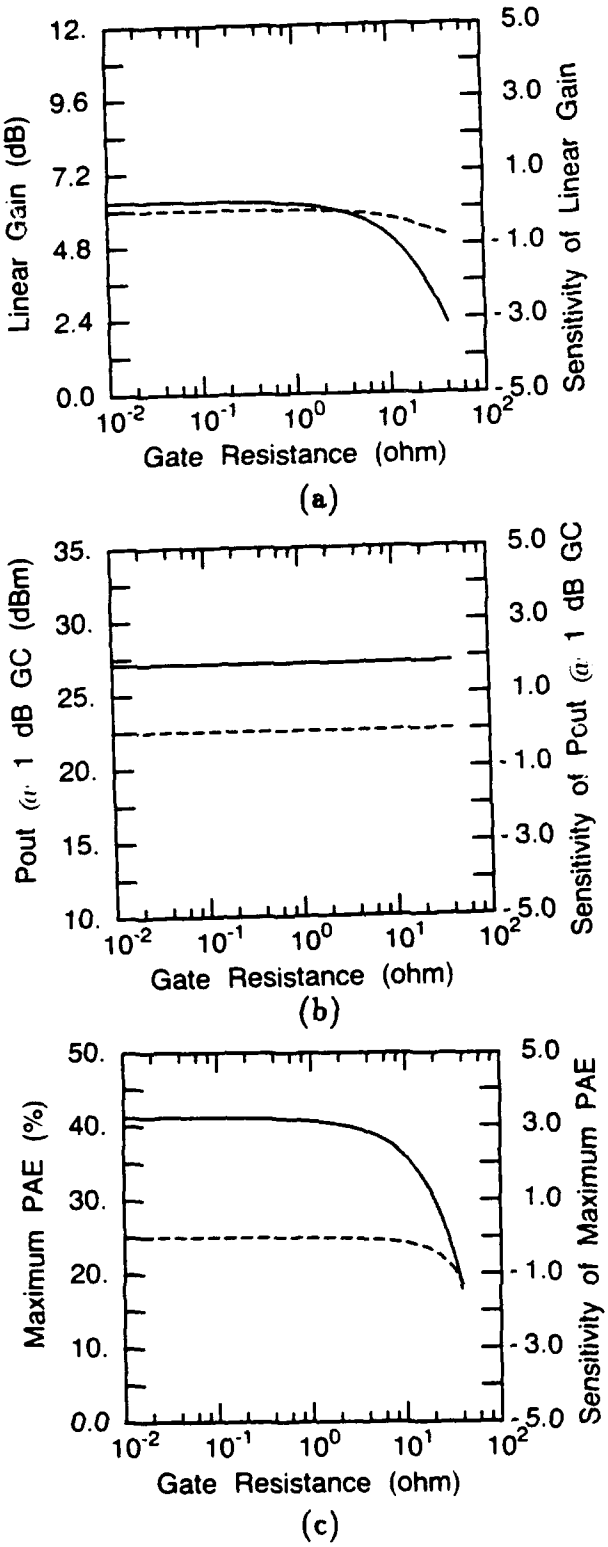


Figure E.7: The effect of parasitic gate resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

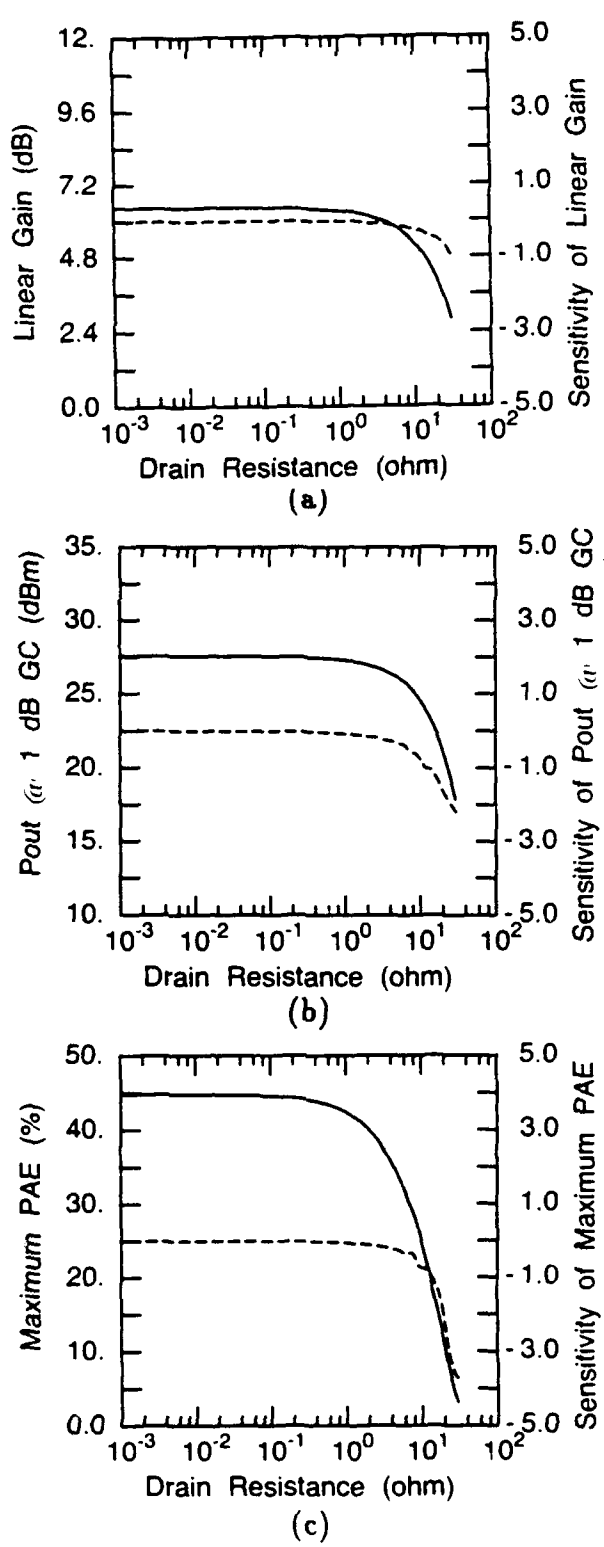


Figure E.8: The effect of parasitic drain resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

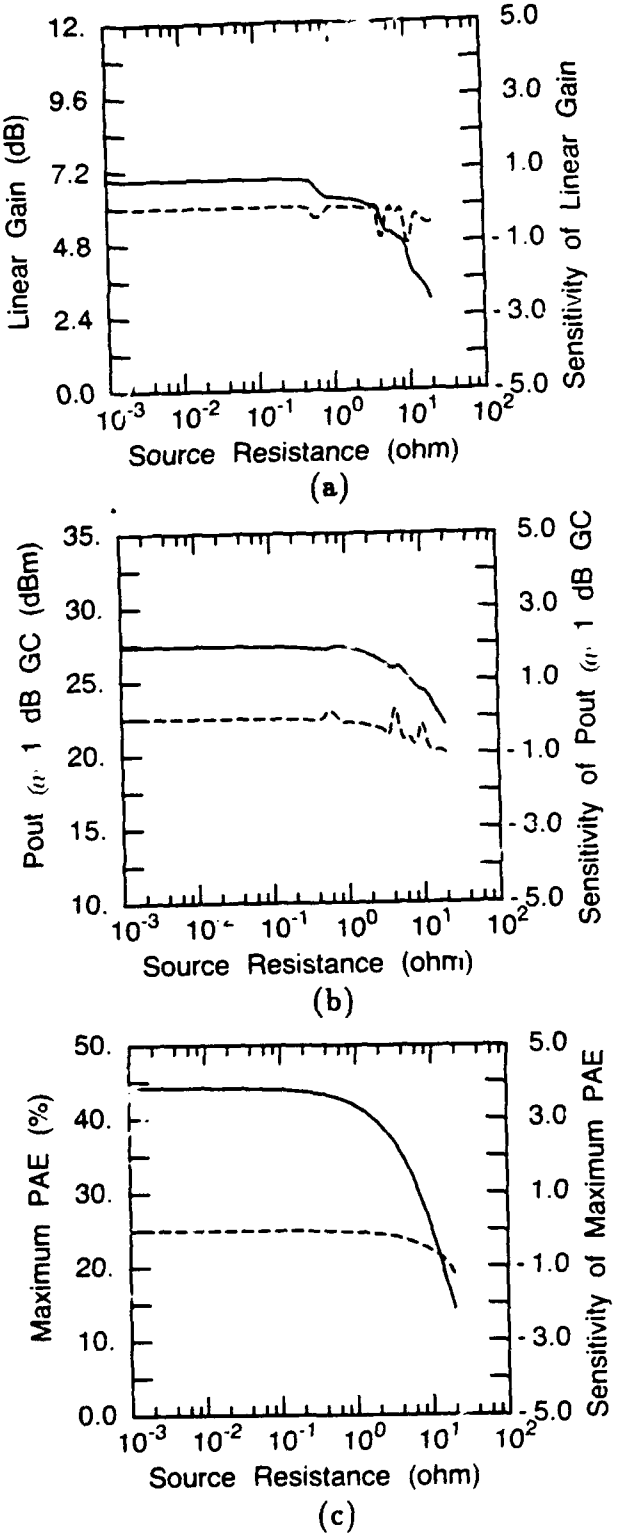


Figure E.9: The effect of parasitic source resistance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

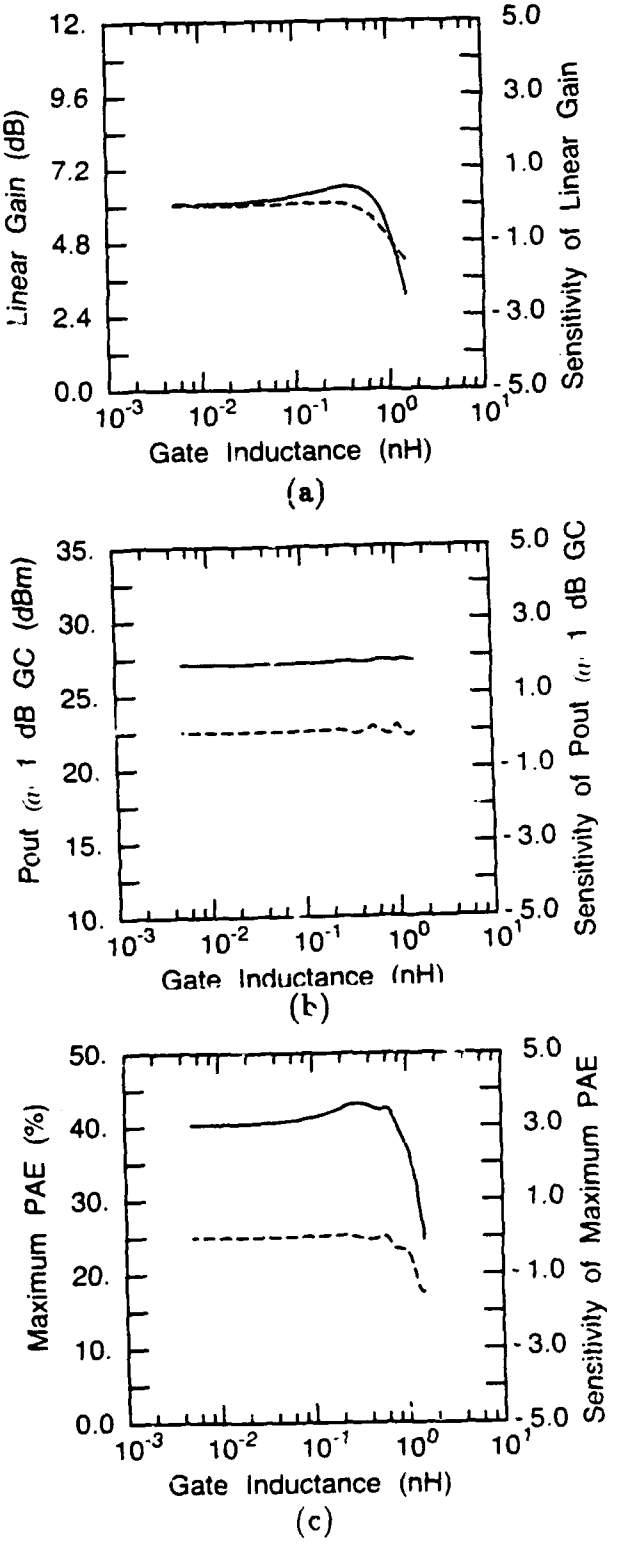
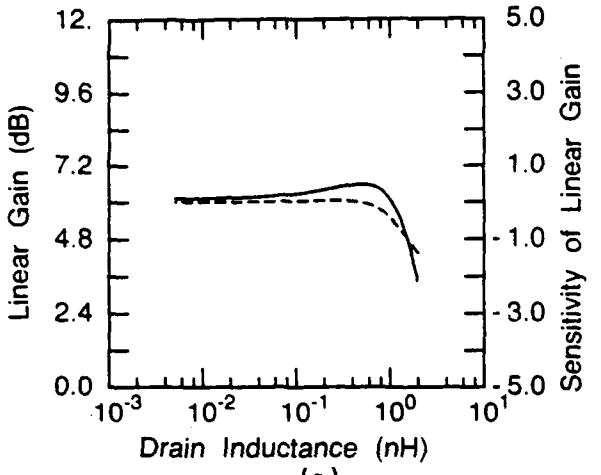
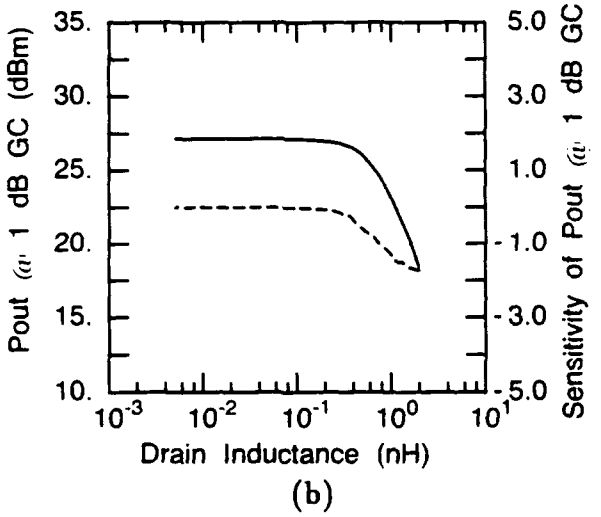


Figure E.10: The effect of parasitic gate inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





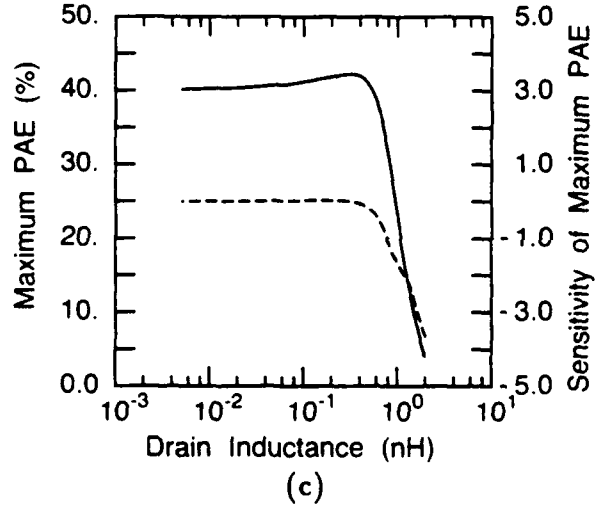
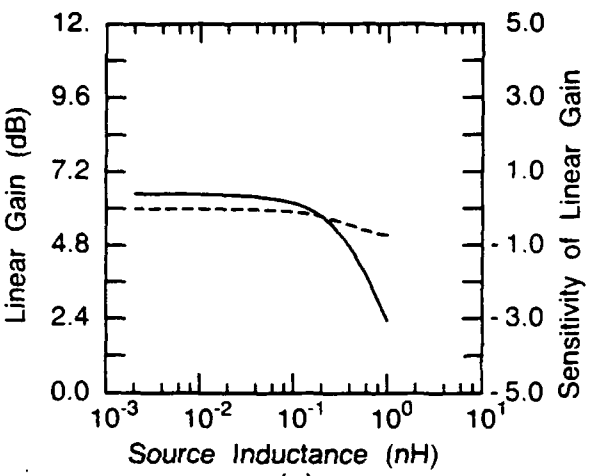
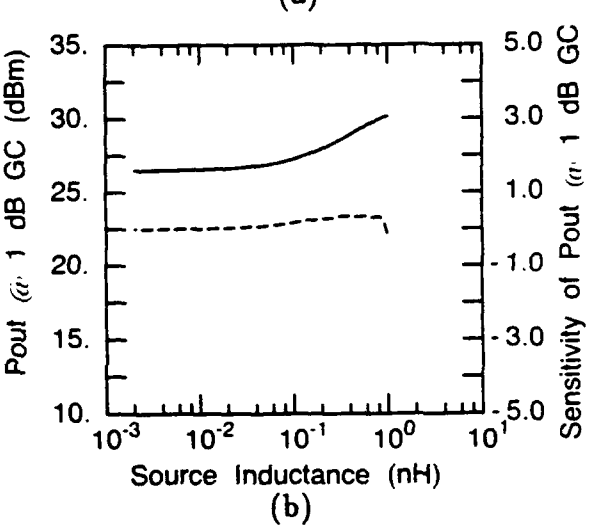


Figure E.11: The effect of parasitic drain inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





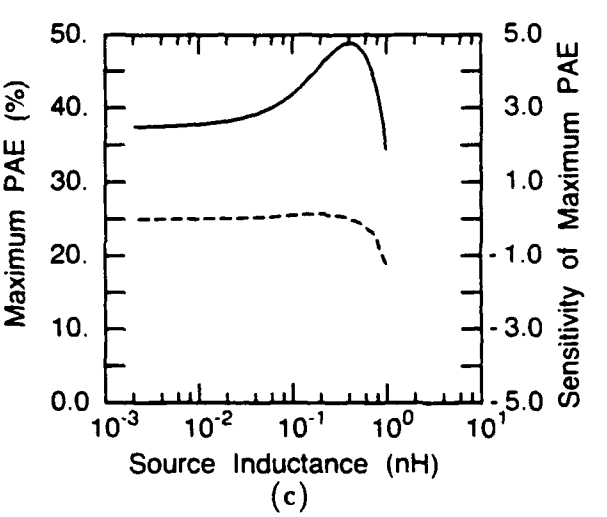
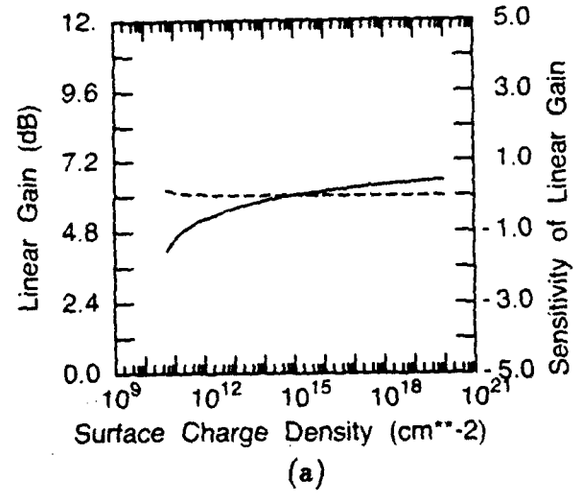
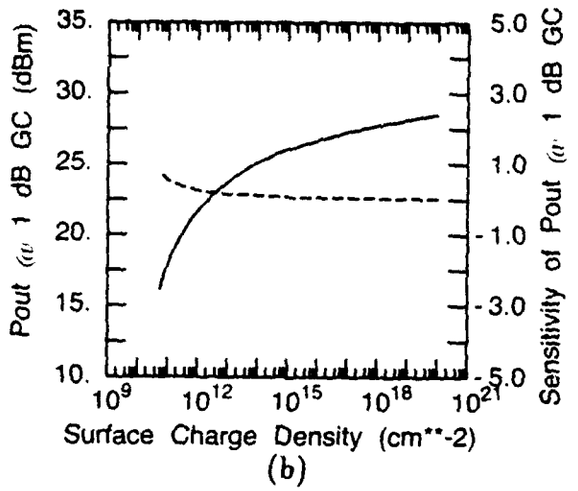


Figure E.12: The effect of parasitic source inductance variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





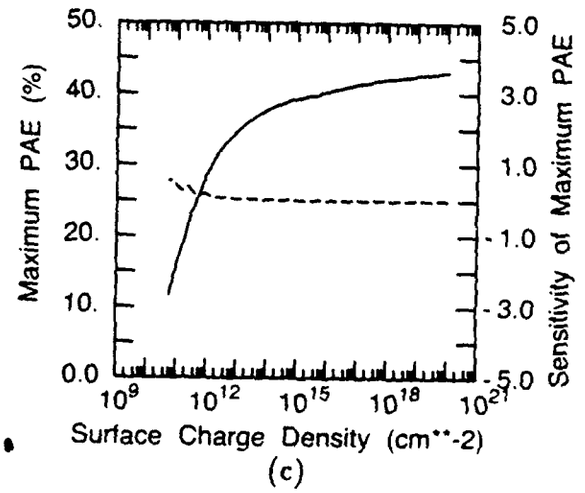
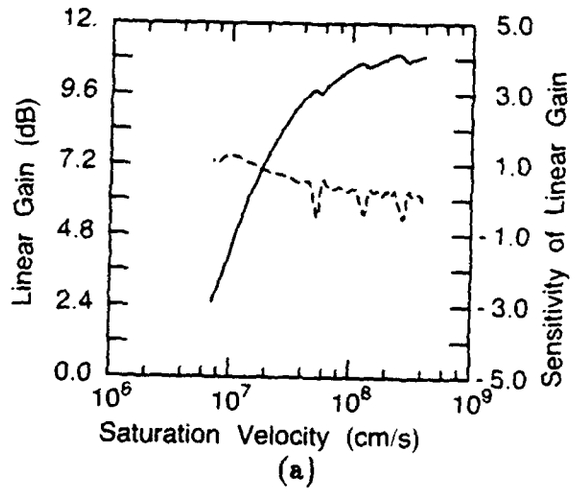
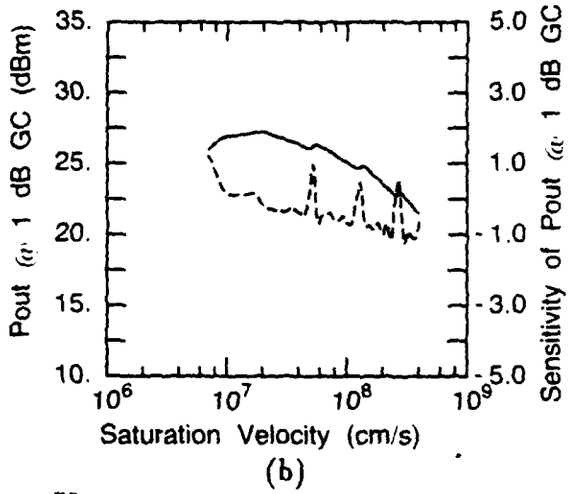


Figure E.13: The effect of surface charge density variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





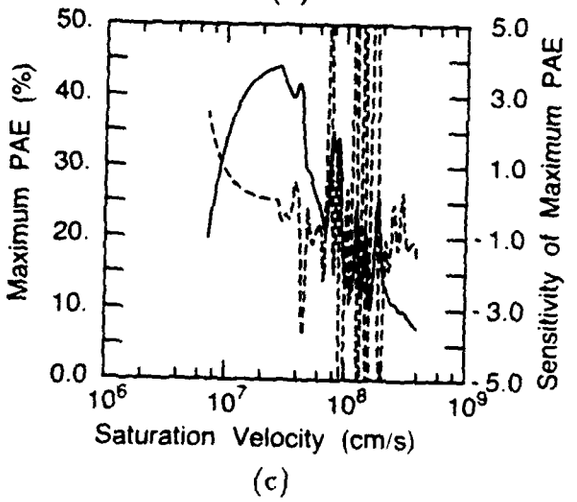


Figure E.14: The effect of electron saturation velocity variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

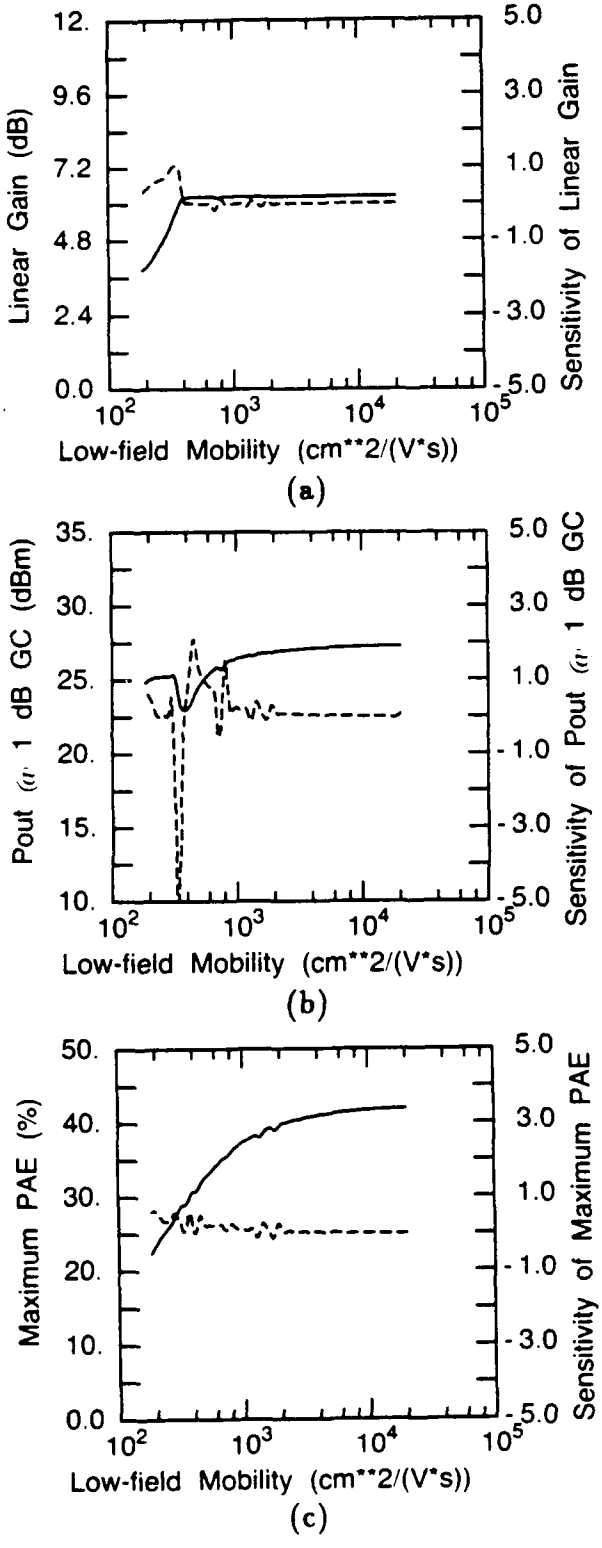


Figure E.15: The effect of electron low-field mobility variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

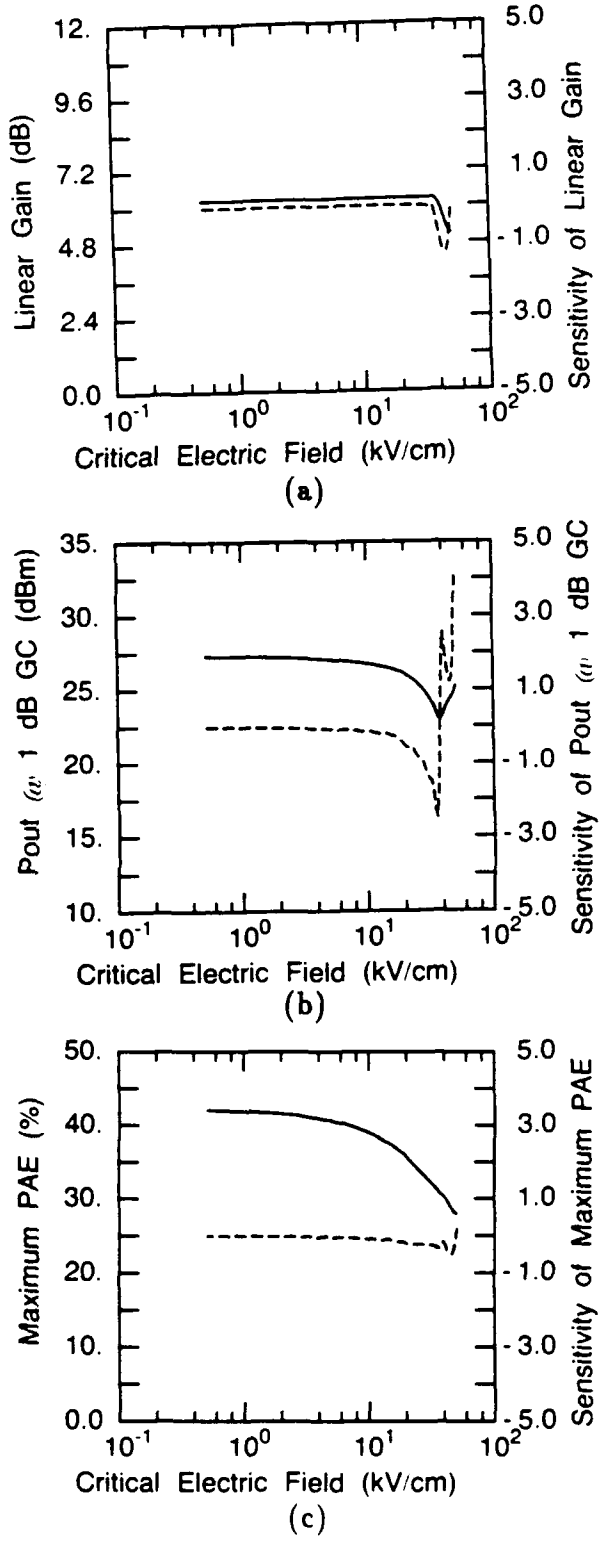
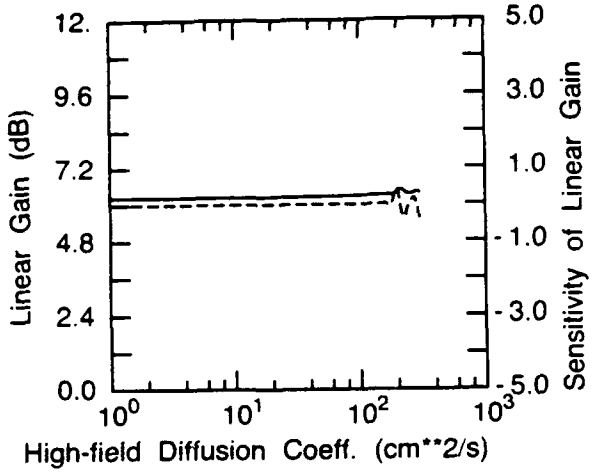
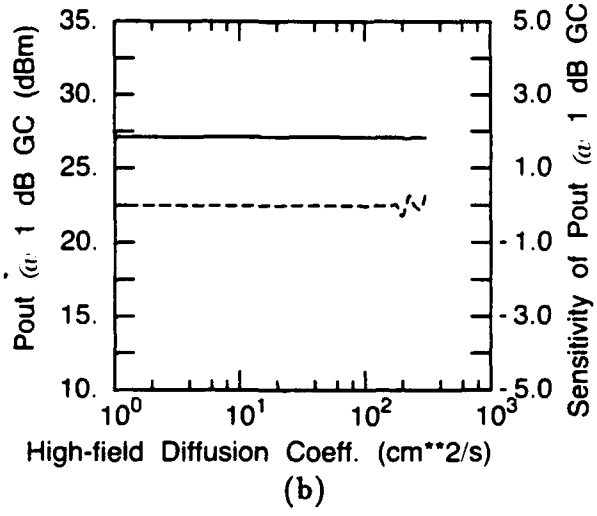


Figure E.16: The effect of electron critical electric field variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





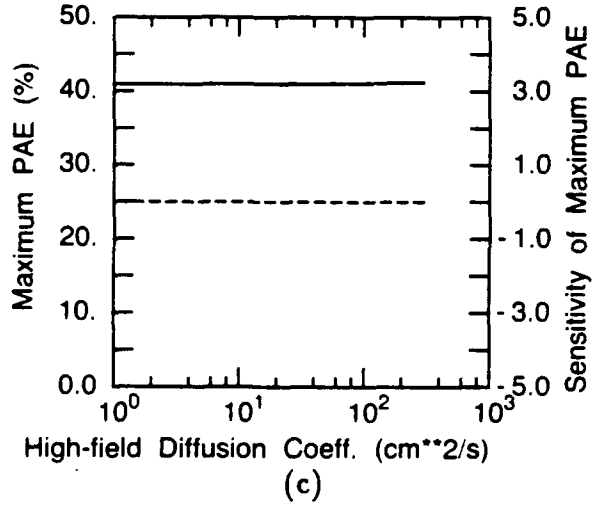
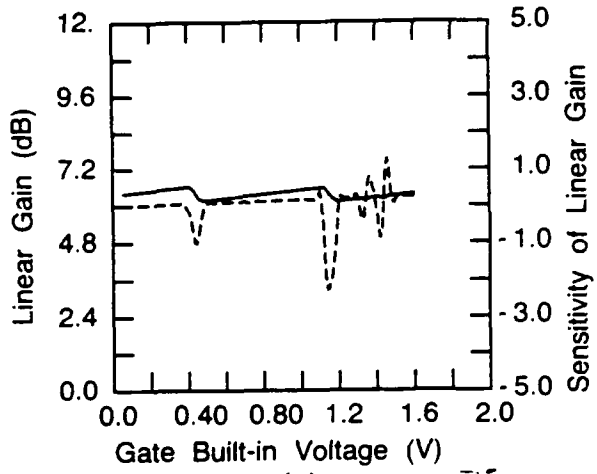
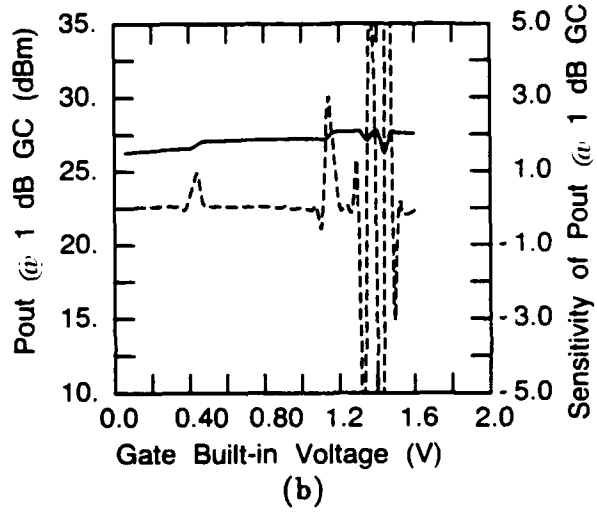


Figure E.17: The effect of electron high-field diffusion coefficient variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.





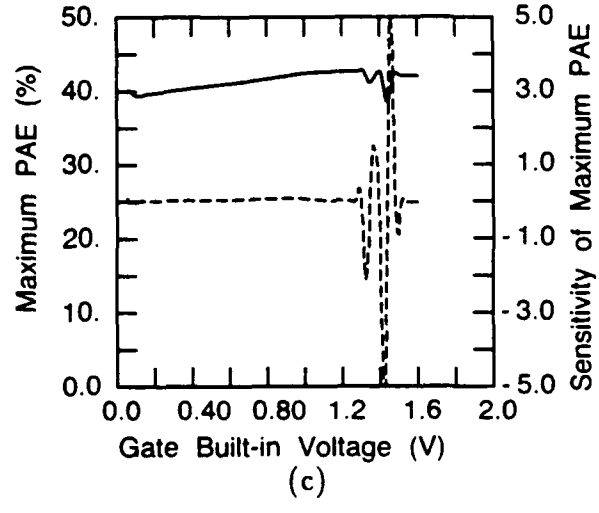


Figure E.18: The effect of gate built-in voltage variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.

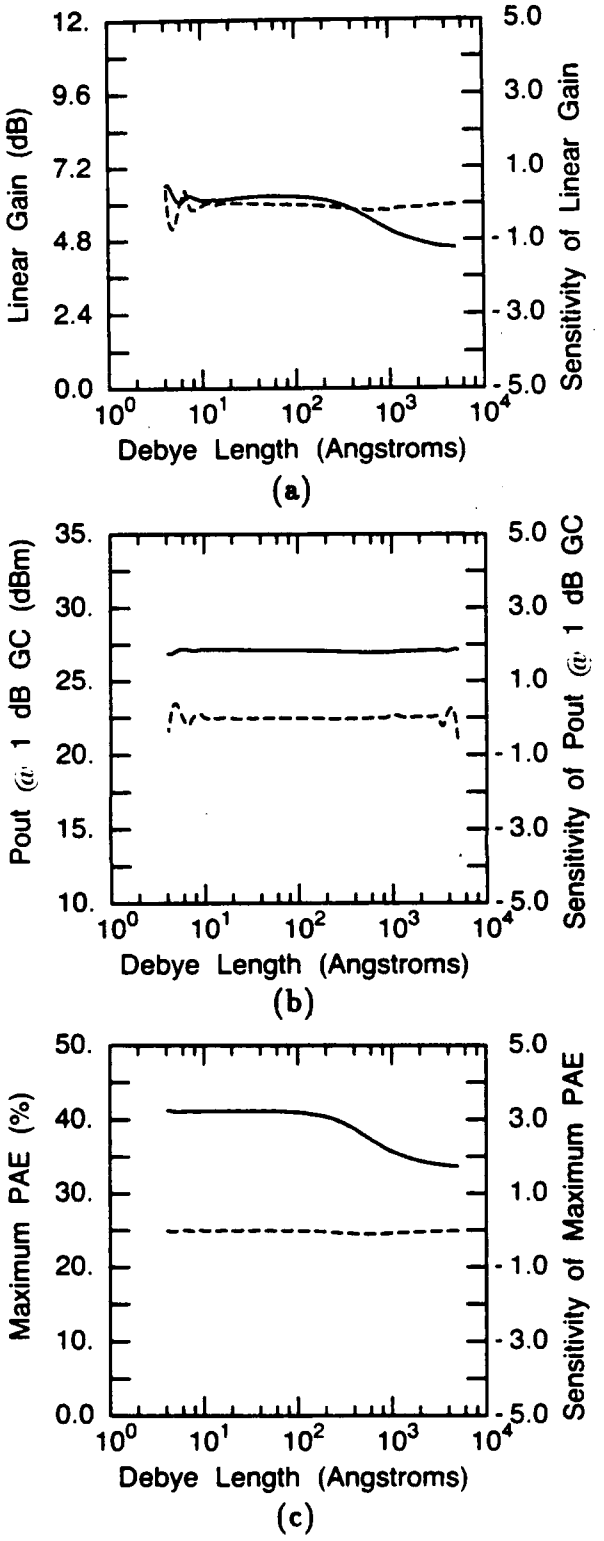


Figure E.19: The effect of Debye length variation on: (a) small-signal transducer gain, (b) output power at 1 dB gain compression, and (c) maximum power-added efficiency.